DATA SHEET

(DOC No. HX8352-A(T)-DS)

HX8352-A (T)

240RGB x 480 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Version 05 December, 2008

Himax Technologies, Inc.
http://www.himax.com.tw

List of Contents

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1. General Description **8**
2. Features **9**
2.1 Display 9
2.2 Display module 9
2.3 Display/control interface 9
2.4 Miscellaneous 10
3. Block Diagram **11**
4. Pin Description **12**
4.1 Pin description 12
4.2 Pin assignment 16
4.3 PAD coordinates 17
4.4 Alignment mark 25
4.5 Bump size 26
5. Function Description **29**
5.1 Interface control mode 29
5.1.1 Register-content interface mode 30
5.1.2 Parallel bus system interface 31
5.1.3 Serial bus system interface 40
5.1.4 RGB interface 42
5.2 Address counter (AC) 45
5.2.1 MCU to memory write/read direction 46
5.3 Source, gate and memory map 48
5.4 Tearing effect output line 49
5.4.1 Tearing effect line modes 49
5.4.2 Tearing effect line timing 50
5.5 Oscillator 53
5.6 Source driver 53
5.7 Gate driver 53
5.8 LCD power generation circuit 54
5.8.1 LCD power generation scheme 54
5.8.2 Various boosting steps 55
5.9 Gamma adjustment 56
5.9.1 Gray voltage generator for source driver 57
5.9.2 Gray voltage generator for digital gamma correction 68
5.10 Scan mode setting 75
5.11 Register setting flow 76
5.12 Power supply setting 78
5.13 OTP programming 79
5.14 Free running mode specification 82
6. Command **85**
6.1 Command set 85
6.2 Index register 87
6.3 Producet ID register (R00h) 87
6.4 Display mode control register (R01h) 87
6.5 Column address start register (R02~03h) 88
6.6 Column address end register (R04~05h) 88
6.7 Row address start register (R06~07h) 88
6.8 Row address end register (R08~09h) 89
6.9 Partial area start row register (R0A~0Bh) 89
6.10 Partial area end row register (R0C~0Dh) 90
6.11 Vertical scroll top fixed area register (R0E~0Fh) 91
6.12 Vertical scroll height area register (R10~11h) 91
6.13 Vertical scroll button fixed area register (R12~13h) 91
6.14 Vertical scroll start address register (R14~15h) 92
6.15 Memory access control register (R16h) 94
6.16 OSC control 1 register (R17h) 95

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List of Contents

6.17 OSC control 2 register (R18h) 95
6.18 Power control 1 register (R19h) 96
6.19 Power control 2 register (R1Ah) 97
6.20 Power control 3 register (R1Bh) 98
6.21 Power control 4 register (R1Ch) 99
6.22 Power control 5 register (R1Dh) 100
6.23 Power control 6 register (R1Eh) 100
6.24 VCOM control register (R1Fh) 102
6.25 Read data register (R22h) 104
6.26 Display control 1 register (R23h) 105
6.27 Display control 2 register (R24h) 106
6.28 Display control 3~8 register (R25h~R2Ah) 107
6.29 Cycle control 1~3 register (R2B~2Dh) 109
6.30 Cycle control 4~8 register (R2E~32h) 110
6.31 Cycle control 10 register (R34h) 112
6.32 Cycle control 11 register (R35h) 112
6.33 Cycle control 12 register (R36h) 113
6.34 Cycle control 13~15 register (R37h~39h) 113
6.35 Interface control 1 register (R3Ah) 114
6.36 Source control 1~2 register (R3Ch~3Dh) 115
6.37 GAMMA control 1~12 register (R3E~49h) 116
6.38 Panel control register (R55h) 119
6.39 OTP related register 1 (R56h) 119
6.40 OTP related register 2 (R57h) 120
6.41 OTP related register 3 (R58h) 120
6.42 OTP related register 4 (R59h) 120
6.43 IP control register (R5Ah) 121
6.44 DGC LUT register (R5Ch) 121
6.45 Test mode control register (R83h) 122
6.46 VDDD control register (R85h) 122
6.47 Power driving control register (R8Ah) 123
6.48 Source gamma resistor setting register (R8B~R8Ch) 123
6.49 SYNC function register (R91h) 124
6.50 PWM control 1 register (R95h) 124
6.51 PWM control 2 register (R96h) 124
6.52 PWM control 3 register (R97h) 125
6.53 CABC PWM period control 1 register (R6Bh) 126
6.54 CABC PWM period control 2 register (R6Ch) 126
6.55 CABC gain setting register (R6Fh ~ R77h) 126
7. Electrical Characteristic **128**
7.1 Absolute maximum ratings 128
7.2 ESD protection level 128
7.3 Latch-up protection level 128
7.4 Light sensitivity 128
7.5 Maximum series resistance 129
7.6 DC characteristics 130
7.7 AC characteristics 131
7.7.1 Parallel interface characteristics (8080-series MPU) 131
7.7.2 Parallel interface characteristics (6800-series MPU) 133
7.7.3 Serial interface characteristics 134
7.7.4 RGB interface characteristics 135
7.7.5 Reset input timing 137
8. Reference Applications **138**
8.1 Register- content interface mode 138

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List of Contents

8.2 External components connection 139
9. Ordering Information 140
10. Revision History 140

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List of Figures

Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)..... 31
Figure 5. 2 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for I80 Series MPU)..... 32
Figure 5. 3 GRAM Read/Write Timing in 8-Bit Parallel Bus System Interface (for I80 Series MPU) 33
Figure 5. 4 Register Read/Write Timing in Parallel Bus System Interface (for M68 Series MPU).... 34
Figure 5. 5 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for M68 Series MPU)..... 35
Figure 5. 6 GRAM Read/Write Timing in 8-bit Parallel Bus System Interface (for M68 Series MPU) 36
Figure 5. 7 Example of I80- / M68- System 16-Bit Parallel Bus Interface..... 37
Figure 5. 8 Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface ("BS2, BS1, BS0"="010") 37
Figure 5. 9 Example of I80- / M68- System 16-bit Parallel Bus Interface..... 38
Figure 5. 10 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input ("BS2, BS1, BS0"="000") 38
Figure 5. 11 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input ("BS2, BS1, BS0"="001") 38
Figure 5. 12 Example of I80- / M68- System 8-Bit Parallel Bus Interface..... 39
Figure 5. 13 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18(6 + 6 + 6) Bit-Data Input ("BS2, BS1, BS0"="011") 39
Figure 5. 14 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 16(5 + 6 + 5) Bit-Data Input ("BS2, BS1, BS0"="100") 39
Figure 5. 15 Data Write Timing in Serial Bus System Interface..... 41
Figure 5. 16 Data Write Timing in Serial Bus System Interface..... 41
Figure 5. 17 RGB Interface Circuit Input Timing 42
Figure 5. 18 16-Bit / Pixel Data Input of RGB Interface 43
Figure 5. 19 18-Bit / Pixel Data Input of RGB Interface 44
Figure 5. 20 MCU to Memory Write/Read Direction 46
Figure 5. 21 MY, MX, MV Setting of 240RGB x 432 Dot 46
Figure 5. 22 Address Direction Settings..... 47
Figure 5. 23 Memory Map (240RGBx432)..... 48
Figure 5. 24 TE Mode 1 Output..... 49
Figure 5. 25 TE Mode 2 Output..... 49
Figure 5. 26 TE Output Waveform 49
Figure 5. 27 Tearing Effect Signal Output..... 50
Figure 5. 28 AC Characteristics of Tearing Effect Signal..... 50
Figure 5. 29 51
Figure 5. 30 51
Figure 5. 31 52
Figure 5. 32 52
Figure 5. 33 Oscillation Circuit 53
Figure 5. 34 LCD Power Generation Scheme 54
Figure 5. 35 Various Boosting Steps..... 55
Figure 5. 36 Gamma Adjustments Different of Source Driver with Digital Gamma Correction..... 56
Figure 5. 37 Grayscale Control 57
Figure 5. 38 Structure of Grayscale Voltage Generator..... 58
Figure 5. 39 Gamma Resister Stream and Gamma Reference Voltage 61
Figure 5. 40 Relationship between Source Output and Vcom..... 67
Figure 5. 41 Relationships between GRAM Data and Output Level..... 67
Figure 5. 42 Block Diagram of Digital Gamma Correction..... 68
Figure 5. 43 Scan Function (240RGB x 432 Dot) 75
Figure 5. 44 Display On/Off Set Sequence..... 76
Figure 5. 45 Standby Mode Setting Sequence 77
Figure 5. 46 Power Supply Setting Flow..... 78
Figure 5. 47 OTP Programming Flow 80
Figure 5. 48 Power On Sequence of FR-mode (for Normally–White Panel) 83

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Figure 5. 49 Power Off Sequence of FR-mode 83

Figure 6. 1 Index Register 87
Figure 6. 2 Product ID Register (R00h) 87
Figure 6. 3 Display Mode Control Register (R01h) 87
Figure 6. 4 Column Address Start Register Upper Byte (R02h) 88
Figure 6. 5 Column Address Start Register Low Byte (R03h) 88
Figure 6. 6 Column Address End Register Upper Byte (R04h) 88
Figure 6. 7 Column Address End Register Low Byte (R05h) 88
Figure 6. 8 Row Address Start Register Upper Byte (R06h) 88
Figure 6. 9 Row Address Start Register Low Byte (R07h) 88
Figure 6. 10 Row Address End Register Upper Byte (R08h) 89
Figure 6. 11 Row Address End Register Low Byte (R09h) 89
Figure 6. 12 Partial Area Start Row Register Upper Byte (R0Ah) 89
Figure 6. 13 Partial Area Start Row Register Low Byte (R0Bh) 89
Figure 6. 14 Partial Area End Row Register Upper Byte (R0Ch) 90
Figure 6. 15 Partial Area End Row Register Low Byte (R0Dh) 90
Figure 6. 16 Vertical Scroll Top Fixed Area Register Upper Byte (R0Eh) 91
Figure 6. 17 Vertical Scroll Top Fixed Area Register Low Byte (R0Fh) 91
Figure 6. 18 Vertical Scroll Height Area Register Upper Byte (R10h) 91
Figure 6. 19 Vertical Scroll Height Area Register Low Byte (R11h) 91
Figure 6. 20 Vertical Scroll Button Fixed Area Register Upper Byte (R12h) 91
Figure 6. 21 Vertical Scroll Button Fixed Area Register Low Byte (R13h) 91
Figure 6. 22 Vertical Scroll Start Address Register Upper Byte (R14h) 92
Figure 6. 23 Vertical Scroll Start Address Register Low Byte (R15h) 92
Figure 6. 24 Memory Access Control Register (R16h) 94
Figure 6. 25 OSC Control 1 Register (R17h) 95
Figure 6. 26 OSC Control 2 Register (R18h) 95
Figure 6. 27 Power Control 1 Register (R19h) 96
Figure 6. 28 Power Control 2 Register (R1Ah) 97
Figure 6. 29 Power Control 3 Register (R1Bh) 98
Figure 6. 30 Power Control 4 Register (R1Ch) 99
Figure 6. 31 Power Control 5 Register (R1Dh) 100
Figure 6. 32 Power Control 6 Register (R1Eh) 100
Figure 6. 33 VCOM Control Register (R1Fh) 102
Figure 6. 34 Read Data Register (R22h) 104
Figure 6. 35 Write Data Register (R22h) 104
Figure 6. 36 Display Control Register (R23h) 105
Figure 6. 37 Display Control 2 Register (R24h) 106
Figure 6. 38 Display Control 2 Register (R25h) 107
Figure 6. 39 Display Control 3 Register (R26h) 107
Figure 6. 40 Display Control 4 Register (R27h) 107
Figure 6. 41 Display Control 5 Register (R28h) 107
Figure 6. 42 Display Control 6 Register (R29h) 107
Figure 6. 43 Display Control 7 Register (R2Ah) 107
Figure 6. 44 Cycle Control 1 Register (R2Bh) 109
Figure 6. 45 Cycle Control 2 Register (R2Ch) 109
Figure 6. 46 Cycle Control 3 Register (R2Dh) 109
Figure 6. 47 Cycle Control 4 Register (R2Eh) 110
Figure 6. 48 Cycle Control 5 Register (R2Fh) 110
Figure 6. 49 Cycle Control 1 Register (R30h) 110
Figure 6. 50 Cycle Control 2 Register (R31h) 110
Figure 6. 51 Cycle Control 3 Register (R32h) 110
Figure 6. 52 Cycle Control 10 Register (R34h) 112
Figure 6. 53 Cycle Control 11 Register (R35h) 112

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List of Figures

Figure 6. 54 Cycle Control 12 Register (R36h) 113
Figure 6. 55 Display Control 5 Register (R37h) 113
Figure 6. 56 Display Control 6 Register (R38h) 113
Figure 6. 57 Display Control 3 Register (R39h) 114
Figure 6. 58 Interface Control 1 Register (R3Ah) 114
Figure 6. 59 Source Control 1 Register (R3Ch) 115
Figure 6. 60 Source Control 2 Register (R3Dh) 115
Figure 6. 61 GAMMA Control 1 Register (R3Eh) 116
Figure 6. 62 GAMMA Control 2 Register (R3Fh) 116
Figure 6. 63 GAMMA Control 3 Register (R40h) 116
Figure 6. 64 GAMMA Control 4 Register (R41h) 116
Figure 6. 65 GAMMA Control 5 Register (R42h) 116
Figure 6. 66 GAMMA Control 6 Register (R43h) 117
Figure 6. 67 GAMMA Control 7 Register (R44h) 117
Figure 6. 68 GAMMA Control8 Register (R45h) 117
Figure 6. 69 GAMMA Control 9 Register (R46h) 117
Figure 6. 70 GAMMA Control 10 Register (R47h) 117
Figure 6. 71 GAMMA Control 11 Register (R48h) 117
Figure 6. 72 GAMMA Control 12 Register (R49h) 117
Figure 6. 73 Panel Control Register (R55h) 119
Figure 6. 74 OTP Related Register 1 (R56h) 119
Figure 6. 75 OTP Related Register 1 (R57h) 120
Figure 6. 76 OTP Related Register 3 (R58h) 120
Figure 6. 77 OTP Related Register 4 (R59h) 120
Figure 6. 78 IP Control Register (R5Ah) 121
Figure 6. 79 DGC LUT WRITE Register (R5Ch) 121
Figure 6. 80 TEST MODE Control Register (R83h) 122
Figure 6. 81 VDDD Control Register (R85h) 122
Figure 6. 82 Power driving control register (R8Ah) 123
Figure 6. 83 Serial Bus Interface Control Register (R8Bh) 123
Figure 6. 84 Serial Bus Interface Control Register (R8Ch) 123
Figure 6. 85 SYNC Function Register (R91h) 124
Figure 6. 86 PWM Control 1 Register (R95h) 124
Figure 6. 87 PWM Control 2 Register (R96h) 124
Figure 6. 88 CABC PWM Period Control 1 Register (R6Bh) 125
Figure 6. 89 CABC PWM Period Control 2 Register (R6Ch) 125
Figure 6. 90 CABC Gain setting Register (R6Fh) 126
Figure 6. 91 CABC Gain setting Register (R70h) 126
Figure 6. 92 CABC Gain setting Register (R71h) 126
Figure 6. 93 CABC Gain setting Register (R72h) 126
Figure 6. 94 CABC Gain setting Register (R73h) 126
Figure 6. 95 CABC Gain setting Register (R74h) 126
Figure 6. 96 CABC Gain setting Register (R75h) 126
Figure 6. 97 CABC Gain setting Register (R76h) 127
Figure 6. 98 CABC Gain setting Register (R77h) 127

Figure 7. 1 Parallel Interface Characteristics (8080-series MPU) 131
Figure 7. 2 Chip Select Timing 132
Figure 7. 3 Write to Read and Read to Write Timing 132
Figure 7. 4 Parallel Interface Characteristics (6800-series MPU) 133
Figure 7. 5 Serial Interface Characteristics 134
Figure 7. 6 RGB Interface Characteristics 135
Figure 7. 7 Reset Input Timing 137

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List of Table

Table 5. 1 Interface Mode Selection 29
Table 5. 2 MPU selection in Register-content Interface Circuit 30
Table 5. 3 Interface Selection in Register-content Interface Mode 30
Table 5. 4 Data Pin Function for I80 Series CPU 31
Table 5. 5 Data Pin Function for M68 Series CPU 31
Table 5. 6 The Function of RS and R/W Bit bus 40
Table 5. 7 EPL Bit Setting and Valid Enable Signal 42
Table 5. 8 Addresses Counter Range 45
Table 5. 9 MY, MX, MV Setting of 240RGB x 432 Dot 46
Table 5. 10 AC Characteristics of Tearing Effect Signal 50
Table 5. 11 Gamma-Adjustment Registers 59
Table 5. 12 Offset Adjustment 0 62
Table 5. 13 Offset Adjustment 1 62
Table 5. 14 Center Adjustment 62
Table 5. 15 Output Voltage of 8 to 1 Selector 62
Table 5. 16 Voltage Calculation Formula (Positive Polarity) 63
Table 5. 17 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity) 64
Table 5. 18 Voltage Calculation Formula (Negative Polarity) 65
Table 5. 19 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity) 66
Table 5. 20 LUT for Red Color (1) 69
Table 5. 21 LUT for Red Color (2) 70
Table 5. 22 LUT for Green Color (1) 71
Table 5. 23 LUT for Green Color (2) 72
Table 5. 24 LUT for Blue Color (1) 73
Table 5. 25 LUT for Blue Color (2) 74
Table 5. 26 OTP Memory Table 79
Table 5. 27 Pin Information of Free Running Mode 82
Table 5. 28 Frequency Definition of Free Running Mode Display 84

Table 7. 1 ESD Protection Level 128
Table 7. 2 129
Table 7. 3 DC Characteristic 130
Table 7. 4 RGB Interface Characteristics 135
Table 7. 5 Vertical and Horizontal Timing for RGB I/F 1375
Table 7. 6 Reset Input Timing 137

Table 8. 1 Connect Capacitors 139
Table 8. 2 Connected Schottky Diode and Resistor 139

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1. General Description

This document describes Himax's HX8352-A is supports four types resolution driving controller. The HX8352-A is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx480 dots at maximum.

The HX8352-A can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, the HX8352-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8352-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

The HX8352-A supports three interface modes, includ Command-Parameter interface mode, Register-Content interface mode. The interface mode is selected by the external pins IFSEL0, P68, BS2~0 setting.

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2. Features

2.1 Display

- Resolution
  - 240(H) x RGB(H) x 480(V)
  - 240(H) x RGB(H) x 432(V)
  - 240(H) x RGB(H) x 400(V)
  - 240(H) x RGB(H) x 320(V)
- Display Color modes
  - Normal Display Mode On
    - 65,536(R(5),G(6),B(5)) colors
    - 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R(1), G(1), B(1)) colors.

2.2 Display module

- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - VLCD = 4.6 to 6.0V (Source output voltage range)
  - VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 240 (H) x 480 (V) x 18 bit

2.3 Display/control interface

- Display Interface types supported
  - 8-/16-/18-bit MPU parallel interface.
  - Serial data transfer interface.
  - 16-/18-data lines parallel video (RGB) interface.
- Control Interface types supported
  - Register-Content interface mode.
- Logic voltage (IOVCC): 1.65 ~ 3.3V
- Logic voltage (VCC): 2.3 ~ 3.3V
- Driver power supply (VCI): 2.3 ~ 3.3V
- Color modes
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6)

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2.4 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support external VDD for lower power consumption (such as 1.8 volts input)
- Support RGB through mode with lower power consumption
- Support Gamma correction of RGB independence
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (one-time-programming) non-volatile memory

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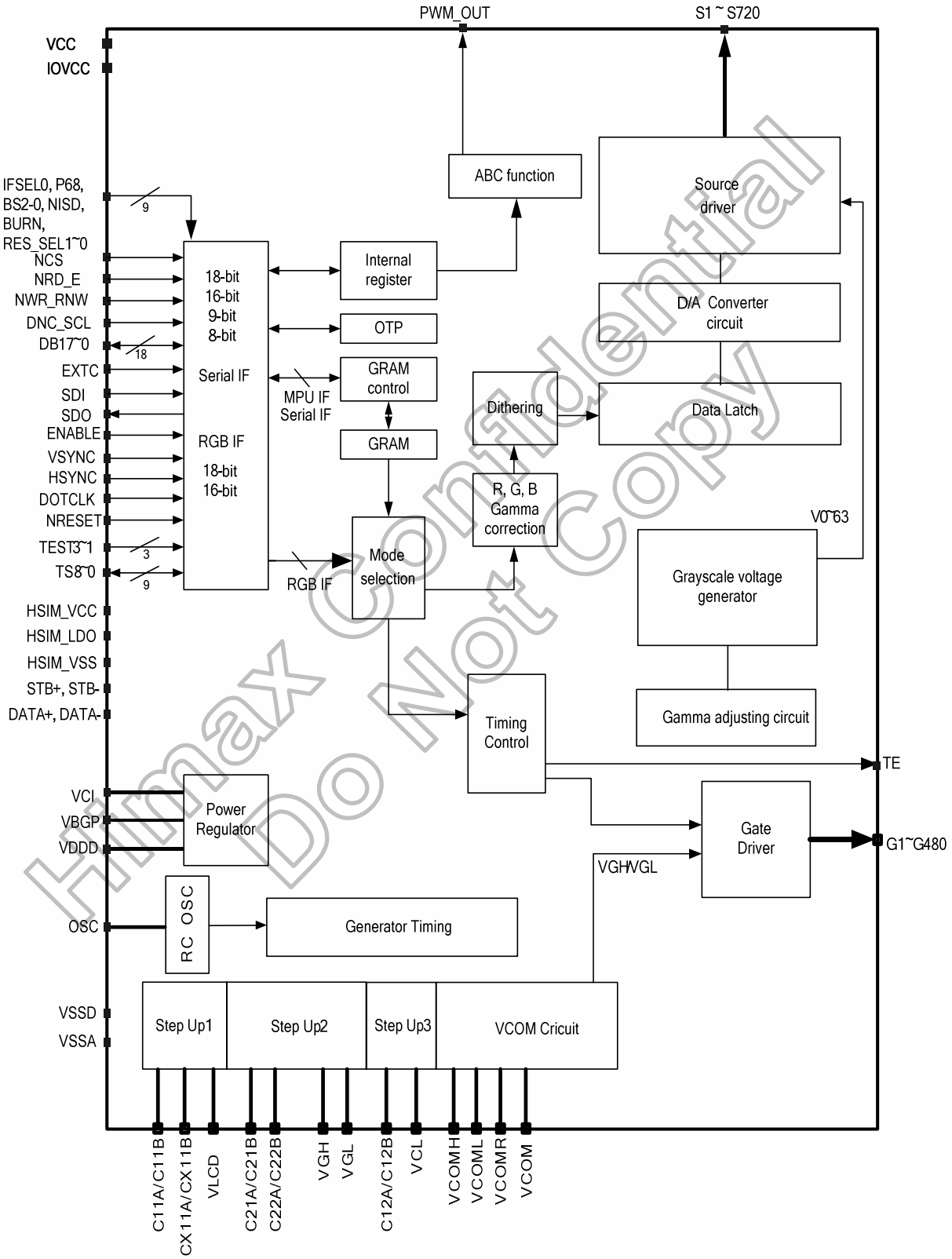
3. Block Diagram



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4. Pin Description

4.1 Pin description

<table>
<tr><th colspan="8">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th colspan="4">Description</th></tr>
<tr><td rowspan="12">P68, BS2,BS1,BS0</td><td rowspan="12">I</td><td rowspan="12">4</td><td rowspan="12">VSSD/ IOVCC</td><td colspan="4">Select the MPU interface mode as listed below
Use with IFSEL0=1 Register-content interface mode.</td></tr>
<tr><td>P68</td><td>BS2</td><td>BS1</td><td>BS0</td><td>Interface mode</td><td>DB pins</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 80-system, 65K-Color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 80-system, 262K-color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface, 80-system, 262K-color</td><td>D17-D0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 80-system, 262K-Color</td><td>D17-D8: Unused D7-D0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 80-system, 65K-Color</td><td>D17-D8: Unused D7-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>16-bit bus interface, 68-system, 65K-Color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-bit bus interface, 68-system, 262K-color</td><td>D17-D16: Unused, D15-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit bus interface, 68-system, 262K-Color</td><td>D17-D0: Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8-bit bus interface, 68-system, 262K-color</td><td>D17-D8:Unused D7-D0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 68-system, 65K-color</td><td>D17-D8:Unused D7-D0: Data</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>ID</td><td>Serial bus IF + RGB interface</td><td>DNC_SCL, SDO,SDI, VSYNC, HSYNC, ENABLE, DOTCLK, DB17-0</td></tr>
<tr><td>IFSEL0</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Interface format select pin
<table><tr><th>IFSEL0</th><th>Interface Format Selection</th></tr><tr><td>0</td><td>Command-Parameter interface mode</td></tr><tr><td>1</td><td>Register-content interface mode</td></tr></table>In this case, the IFSEL0 has to be connected to IOVCC.</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">When operate in Register-content interface mode, the EXTC has to be connected to IOVCC or VSSD.</td></tr>
<tr><td>RES_SEL1~0</td><td>I</td><td>2</td><td>MPU</td><td colspan="4">Panel Resolution select pin.
<table><tr><th>RES_SEL1</th><th>RES_SEL0</th><th>Panel Resolution</th><th>Connection of Gate</th></tr><tr><td>0</td><td>0</td><td>240RGB x 320 dot</td><td>G1 ~ G320</td></tr><tr><td>0</td><td>1</td><td>240RGB x 400 dot</td><td>G1 ~ G400</td></tr><tr><td>1</td><td>0</td><td>240RGB x 432 dot</td><td>G1 ~ G432</td></tr><tr><td>1</td><td>1</td><td>240RGB x 480 dot</td><td>G1 ~ G480</td></tr></table></td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
Must be connected to VSSD if not in use.</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">I80 system: Serves as a write signal and writes data at the rising edge.
M68 system: 0: Write, 1: Read.
Fix it to IOVCC or VSSD level when using serial bus interface.</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">I80 system: Serves as a read signal and read data at the low level.
M68 system: 0: Read/Write disable, 1: Read/Write enable.
Fix it to IOVCC or VSSD level when using serial bus interface.</td></tr>
<tr><td>DNC_SCL</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">The signal for command or parameter select under parallel mode(i.e. Not serial interface):
Low: command, High: parameter.
When under serial interface, it servers as SCL.</td></tr>
<tr><td>BURN</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Free Running mode
If BURN=Hi, this can enable free running mode for burn in test.
The display data alternates between full black and full white independent of input data in free running mode.</td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td colspan="4">Serial data input. If not used, please let it connected to IOVCC or VSSD.</td></tr>
</table>

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Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VSYNC	I	1	MPU	Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.
HSYNC	I	1	MPU	Frame synchronizing signal. Has to be fixed to IOVCC level if is not used.
ENABLE	I	1	MPU	A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level if unused (High active, if EPL=0).
DOTCLK	I	1	MPU	Dot clock signal. Has to be fixed to VSSD level if is not used.
NRESET	I	8	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
OSC	I	1	Oscillation Resistor	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
VCOMR	I	2	Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8352-A.
VGS	I	2	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G480	O	480	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	7	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	2	MPU	Tearing effect output. If not used, please open this pin.
SDO	O	2	MPU	Serial data output. If not use, let it to open.
NISD	O	2	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL, Source and VCOM would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.
PWM_OUT	O	2	External LED driver IC	Backlight On/Off control pin. If use ABC function, the pin can connect to external LED driver IC. The output voltage rage = 0~ IOVCC.
NWR2	O	2	Sub Panel	80-interface NWR signal output pin for Sub Panel
E2	O	2	Sub Panel	68-interface Enable signal output pin for Sub Panel
NCS2	O	2	Sub Panel	The signal is Chip select for Sub Panel.
RS2	O	2	Sub Panel	The signal is register index or register parameter select for Sub Panel

HSIM Interface Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
STB+, STB-	-	2 2	HSIM Host	High Speed Interface Strobe differential signal input pins. STB+ pin for Strobe+, STB- pin for Strobe-. Connect to a terminal resistance (100Ω) between STB+ and STB-. If not used, please let it connected to VSSD.
DATA+, DATA-	-	2 2	HSIM Host	High Speed Interface Data differential signal input pins. DATA+ pin for Data+, DATA- pin for Data-. Connect to a terminal resistance (100Ω) between DATA+ and DATA-. If not used, please let it connected to VSSD.
HSIM_VCC	P	8	Power Supply	High Speed Interface I/O power supply pin, 2.3V~3.3V.
HSIM_VSS	P	6	Ground	High Speed Interface I/O ground pin.

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HSIM_LDO	O	1	Capacitor	High Speed Interface regulator output pin. Connect to a stabilizing capacitor between HSIM_VSS and HSIM_LDO If not used, please open these pins.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B CX11A, CX11B	I/O	10,10 10,10	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B	I/O	8,8	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 2 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	12,12 12,12	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
DB17~0/ PD17~0 (DBS17~0)	I/O	36	MPU	When Operates in system interface mode, it is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 When Operation in RGB interface mode, it is an 18-bit bus RGB data bus. If not used, please open these pins.
GPIO7~0	I/O	16	-	Standard Input/Output pin As for GPIO7 to 0 terminal, setting of an input and output direction is possible. If not used, please open these pins.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	9	Power Supply	Digital IO Pad power supply, 1.65V~3.3V
VCC	P	2	Power Supply	Digital power supply, 2.3V~3.3V
VCI	P	6	Power Supply	Analog power supply, 2.3V~3.3V
VSSD	P	13	Ground	Digital ground
VSSA	P	13	Ground	Analog ground
VDDD	O	16	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
REGVDD	I	1	MPU	If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the voltage range 1.65~1.95V. Must be connected to IOVCC or VSSD.
VBGP	-	2	Open	Band Gap Voltage. Let it to be open.
VREG1	P	4	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VREG3	P	4	Stabilizing Capacitor	A reference voltage for VGH&VGL.
VCOMH	P	4	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	7	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.

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Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCL	P	6	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
VLCD	P	6	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and VLCD. Place a schotkey barrier diode (see “configuration of the power supply”).
VGH	P	6	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH. Place a schottkey barrier diode between VCI and VGH. Place a schottkey barrier diode (see “configuration of the power supply”).
VGL	P	6	Stabilizing capacitor	An output from the step-up circuit2.or –3~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply”).

Test Pin and Others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST3-1	I	3	GND	Test pin input (Internal pull low)
TS8~0	O	18	Open	A test pin. Disconnect it.
VTEST	O	1	Open	A test pin. Disconnect it.
DUMMYR1-2	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.
DUMMYR3-4	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR3 and DUMMYR4 are short-circuited within the chip.
DUMMY	-	99	Open	Dummy pads
IOGNDDUM1-10	O	12	Open	Leave them open.
PADA0,PADB0	I	2	MPU	Test pin for display glass break detection. If not used, please open these pins.
PADA1~ PADA4, PADB1~ PADB4	I	4 4	MPU	Test pin for chip attachment detection. If not used, please open these pins.
DMY_IOVCC	O	10	-	Dummy IOVCC output pads, Internal connected to IOVCC and only for external Hardware setting pin use. If not used, please open these pins.
DMY_GND	O	8	-	Dummy GND output pads, Internal connected to VSSD and only for external Hardware setting pin use. If not used, please open these pins.
TEST_MODE	-	1	Open	A test pin. Disconnect it.
TEST_PAD_DRV	-	1	Open	A test pin. Disconnect it.
TEST_MODE_CLK	-	1	Open	A test pin. Disconnect it.

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4.2 Pin assignment

Chip Size: 18680 um x 1020 um
(Including Seal-ring 20 um *2
Scribe line 40 um *2)

Chip Thickness: 300 um (typ.)

Pad Location: Pad center

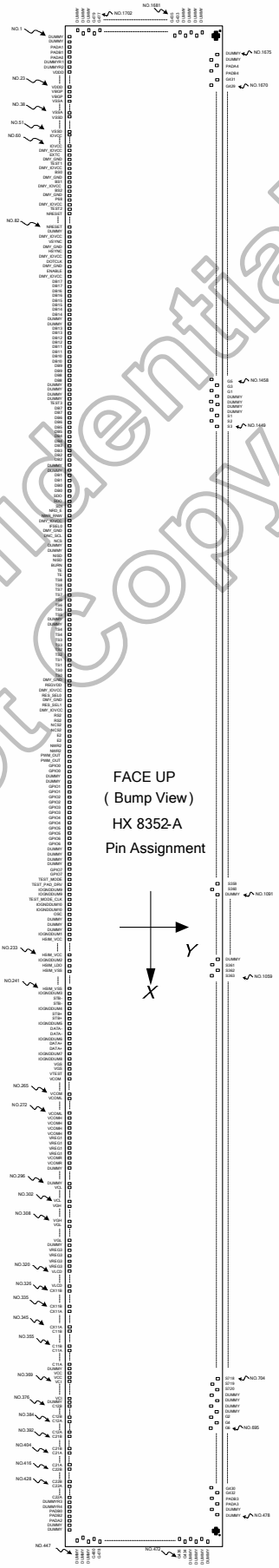
Coordinate Origin: Chip center

Au Bump Size:
1. 24 um x 120 um
   Input/Output
   (No. 1~ No. 446)

2. 106 um x 14 um
   Staggered LCD output side
   (No. 447 ~ No. 477)

3. 14 um x 106 um
   Staggered LCD output side
   (No. 478 ~ No. 1675)

4. 106 um x 14 um
   Staggered LCD output side
   (No. 1676 ~ No. 1706)



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4.3 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-9189	-385	61	DMY_IOVCC	-6789	-385	121	DB7	-4389	-385	181	DMY_IOVCC	-1989	-385
2	DUMMY	-9149	-385	62	EXTC	-6749	-385	122	DB6	-4349	-385	182	RS2	-1949	-385
3	PADA1	-9109	-385	63	DMY_GND	-6709	-385	123	DB6	-4309	-385	183	RS2	-1909	-385
4	PADB1	-9069	-385	64	TEST1	-6669	-385	124	DB5	-4269	-385	184	NCS2	-1869	-385
5	PADA0	-9029	-385	65	DMY_IOVCC	-6629	-385	125	DB5	-4229	-385	185	NCS2	-1829	-385
6	DUMMYR1	-8989	-385	66	BS0	-6589	-385	126	DB4	-4189	-385	186	E2	-1789	-385
7	DUMMYR2	-8949	-385	67	DMY_GND	-6549	-385	127	DB4	-4149	-385	187	E2	-1749	-385
8	VDDD	-8909	-385	68	BS1	-6509	-385	128	DB3	-4109	-385	188	NWR2	-1709	-385
9	VDDD	-8869	-385	69	DMY_IOVCC	-6469	-385	129	DB3	-4069	-385	189	NWR2	-1669	-385
10	VDDD	-8829	-385	70	BS2	-6429	-385	130	DB2	-4029	-385	190	PWM_OUT	-1629	-385
11	VDDD	-8789	-385	71	DMY_GND	-6389	-385	131	DB2	-3989	-385	191	PWM_OUT	-1589	-385
12	VDDD	-8749	-385	72	P68	-6349	-385	132	DUMMY	-3949	-385	192	GPIO0	-1549	-385
13	VDDD	-8709	-385	73	DMY_IOVCC	-6309	-385	133	DUMMY	-3909	-385	193	GPIO0	-1509	-385
14	VDDD	-8669	-385	74	TEST2	-6269	-385	134	DB1	-3869	-385	194	DUMMY	-1469	-385
15	VDDD	-8629	-385	75	NRESET	-6229	-385	135	DB1	-3829	-385	195	DUMMY	-1429	-385
16	VDDD	-8589	-385	76	NRESET	-6189	-385	136	DB0	-3789	-385	196	GPIO1	-1389	-385
17	VDDD	-8549	-385	77	NRESET	-6149	-385	137	DB0	-3749	-385	197	GPIO1	-1349	-385
18	VDDD	-8509	-385	78	NRESET	-6109	-385	138	SDO	-3709	-385	198	GPIO2	-1309	-385
19	VDDD	-8469	-385	79	NRESET	-6069	-385	139	SDO	-3669	-385	199	GPIO2	-1269	-385
20	VDDD	-8429	-385	80	NRESET	-6029	-385	140	SDI	-3629	-385	200	GPIO3	-1229	-385
21	VDDD	-8389	-385	81	NRESET	-5989	-385	141	NRD_E	-3589	-385	201	GPIO3	-1189	-385
22	VDDD	-8349	-385	82	NRESET	-5949	-385	142	NWR_RNW	-3549	-385	202	GPIO4	-1149	-385
23	VDDD	-8309	-385	83	DUMMY	-5909	-385	143	DMY_IOVCC	-3509	-385	203	GPIO4	-1109	-385
24	VBGP	-8269	-385	84	DMY_IOVCC	-5869	-385	144	IFSEL0	-3469	-385	204	GPIO5	-1069	-385
25	VBGP	-8229	-385	85	VSYNC	-5829	-385	145	DMY_GND	-3429	-385	205	GPIO5	-1029	-385
26	VSSA	-8189	-385	86	DMY_GND	-5789	-385	146	DNC_SCL	-3389	-385	206	GPIO6	-989	-385
27	VSSA	-8149	-385	87	HSYNC	-5749	-385	147	NCS	-3349	-385	207	GPIO6	-949	-385
28	VSSA	-8109	-385	88	DMY_IOVCC	-5709	-385	148	DUMMY	-3309	-385	208	DUMMY	-909	-385
29	VSSA	-8069	-385	89	DOTCLK	-5669	-385	149	DUMMY	-3269	-385	209	DUMMY	-869	-385
30	VSSA	-8029	-385	90	DMY_GND	-5629	-385	150	NISD	-3229	-385	210	DUMMY	-829	-385
31	VSSA	-7989	-385	91	ENABLE	-5589	-385	151	NISD	-3189	-385	211	DUMMY	-789	-385
32	VSSA	-7949	-385	92	DMY_IOVCC	-5549	-385	152	BURN	-3149	-385	212	GPIO7	-749	-385
33	VSSA	-7909	-385	93	DB17	-5509	-385	153	TE	-3109	-385	213	GPIO7	-709	-385
34	VSSA	-7869	-385	94	DB17	-5469	-385	154	TE	-3069	-385	214	TEST_MODE	-669	-385
35	VSSA	-7829	-385	95	DB16	-5429	-385	155	TS8	-3029	-385	215	TEST_PAD_DRV	-629	-385
36	VSSA	-7789	-385	96	DB16	-5389	-385	156	TS8	-2989	-385	216	IOGNDDUM9	-589	-385
37	VSSA	-7749	-385	97	DB15	-5349	-385	157	TS7	-2949	-385	217	IOGNDDUM9	-549	-385
38	VSSA	-7709	-385	98	DB15	-5309	-385	158	TS7	-2909	-385	218	TEST_MODE_CLK	-509	-385
39	VSSD	-7669	-385	99	DB14	-5269	-385	159	TS6	-2869	-385	219	IOGNDDUM10	-469	-385
40	VSSD	-7629	-385	100	DB14	-5229	-385	160	TS6	-2829	-385	220	IOGNDDUM10	-429	-385
41	VSSD	-7589	-385	101	DUMMY	-5189	-385	161	TS5	-2789	-385	221	OSC	-389	-385
42	VSSD	-7549	-385	102	DUMMY	-5149	-385	162	TS5	-2749	-385	222	DUMMY	-349	-385
43	VSSD	-7509	-385	103	DB13	-5109	-385	163	DUMMY	-2709	-385	223	DUMMY	-309	-385
44	VSSD	-7469	-385	104	DB13	-5069	-385	164	DUMMY	-2669	-385	224	DUMMY	309	-385
45	VSSD	-7429	-385	105	DB12	-5029	-385	165	TS4	-2629	-385	225	IOGNDDUM1	349	-385
46	VSSD	-7389	-385	106	DB12	-4989	-385	166	TS4	-2589	-385	226	HSIM_VCC	389	-385
47	VSSD	-7349	-385	107	DB11	-4949	-385	167	TS3	-2549	-385	227	HSIM_VCC	429	-385
48	VSSD	-7309	-385	108	DB11	-4909	-385	168	TS3	-2509	-385	228	HSIM_VCC	469	-385
49	VSSD	-7269	-385	109	DB10	-4869	-385	169	TS2	-2469	-385	229	HSIM_VCC	509	-385
50	VSSD	-7229	-385	110	DB10	-4829	-385	170	TS2	-2429	-385	230	HSIM_VCC	549	-385
51	VSSD	-7189	-385	111	DB9	-4789	-385	171	TS1	-2389	-385	231	HSIM_VCC	589	-385
52	IOVCC	-7149	-385	112	DB9	-4749	-385	172	TS1	-2349	-385	232	HSIM_VCC	629	-385
53	IOVCC	-7109	-385	113	DB8	-4709	-385	173	TS0	-2309	-385	233	HSIM_VCC	669	-385
54	IOVCC	-7069	-385	114	DB8	-4669	-385	174	TS0	-2269	-385	234	IOGNDDUM2	709	-385
55	IOVCC	-7029	-385	115	DUMMY	-4629	-385	175	DMY_GND	-2229	-385	235	HSIM_LDO	749	-385
56	IOVCC	-6989	-385	116	DUMMY	-4589	-385	176	REGVDD	-2189	-385	236	HSIM_VSS	789	-385
57	IOVCC	-6949	-385	117	DUMMY	-4549	-385	177	DMY_IOVCC	-2149	-385	237	HSIM_VSS	829	-385
58	IOVCC	-6909	-385	118	DUMMY	-4509	-385	178	RES_SEL0	-2109	-385	238	HSIM_VSS	869	-385
59	IOVCC	-6869	-385	119	TEST3	-4469	-385	179	DMY_GND	-2069	-385	239	HSIM_VSS	909	-385
60	IOVCC	-6829	-385	120	DB7	-4429	-385	180	RES_SEL1	-2029	-385	240	HSIM_VSS	949	-385

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No.	Name	X	Y
241	HSIM_VSS	989	-385
242	IOGNDDUM3	1029	-385
243	STB-	1069	-385
244	STB-	1109	-385
245	IOGNDDUM4	1149	-385
246	STB+	1189	-385
247	STB+	1229	-385
248	IOGNDDUM5	1269	-385
249	DATA-	1309	-385
250	DATA-	1349	-385
251	IOGNDDUM6	1389	-385
252	DATA+	1429	-385
253	DATA+	1469	-385
254	IOGNDDUM7	1509	-385
255	IOGNDDUM8	1549	-385
256	VGS	1589	-385
257	VGS	1629	-385
258	VTEST	1669	-385
259	VCOM	1709	-385
260	VCOM	1749	-385
261	VCOM	1789	-385
262	VCOM	1829	-385
263	VCOM	1869	-385
264	VCOM	1909	-385
265	VCOM	1949	-385
266	VCOML	1989	-385
267	VCOML	2029	-385
268	VCOML	2069	-385
269	VCOML	2109	-385
270	VCOML	2149	-385
271	VCOML	2189	-385
272	VCOML	2229	-385
273	VCOMH	2269	-385
274	VCOMH	2309	-385
275	VCOMH	2349	-385
276	VCOMH	2389	-385
277	VREG1	2429	-385
278	VREG1	2469	-385
279	VREG1	2509	-385
280	VREG1	2549	-385
281	VCOMR	2589	-385
282	VCOMR	2629	-385
283	DUMMY	2669	-385
284	DUMMY	2709	-385
285	DUMMY	2749	-385
286	DUMMY	2789	-385
287	DUMMY	2829	-385
288	DUMMY	2869	-385
289	DUMMY	2909	-385
290	DUMMY	2949	-385
291	DUMMY	2989	-385
292	DUMMY	3029	-385
293	DUMMY	3069	-385
294	DUMMY	3109	-385
295	DUMMY	3149	-385
296	DUMMY	3189	-385
297	VCL	3229	-385
298	VCL	3269	-385
299	VCL	3309	-385
300	VCL	3349	-385

No.	Name	X	Y
301	VCL	3389	-385
302	VCL	3429	-385
303	VGH	3469	-385
304	VGH	3509	-385
305	VGH	3549	-385
306	VGH	3589	-385
307	VGH	3629	-385
308	VGH	3669	-385
309	VGL	3709	-385
310	VGL	3749	-385
311	VGL	3789	-385
312	VGL	3829	-385
313	VGL	3869	-385
314	VGL	3909	-385
315	DUMMY	3949	-385
316	VREG3	3989	-385
317	VREG3	4029	-385
318	VREG3	4069	-385
319	VREG3	4109	-385
320	VLCD	4149	-385
321	VLCD	4189	-385
322	VLCD	4229	-385
323	VLCD	4269	-385
324	VLCD	4309	-385
325	VLCD	4349	-385
326	CX11B	4389	-385
327	CX11B	4429	-385
328	CX11B	4469	-385
329	CX11B	4509	-385
330	CX11B	4549	-385
331	CX11B	4589	-385
332	CX11B	4629	-385
333	CX11B	4669	-385
334	CX11B	4709	-385
335	CX11B	4749	-385
336	CX11A	4789	-385
337	CX11A	4829	-385
338	CX11A	4869	-385
339	CX11A	4909	-385
340	CX11A	4949	-385
341	CX11A	4989	-385
342	CX11A	5029	-385
343	CX11A	5069	-385
344	CX11A	5109	-385
345	CX11A	5149	-385
346	C11B	5189	-385
347	C11B	5229	-385
348	C11B	5269	-385
349	C11B	5309	-385
350	C11B	5349	-385
351	C11B	5389	-385
352	C11B	5429	-385
353	C11B	5469	-385
354	C11B	5509	-385
355	C11B	5549	-385
356	C11A	5589	-385
357	C11A	5629	-385
358	C11A	5669	-385
359	C11A	5709	-385
360	C11A	5749	-385

No.	Name	X	Y
361	C11A	5789	-385
362	C11A	5829	-385
363	C11A	5869	-385
364	C11A	5909	-385
365	C11A	5949	-385
366	DUMMY	5989	-385
367	VCC	6029	-385
368	VCC	6069	-385
369	VCI	6109	-385
370	VCI	6149	-385
371	VCI	6189	-385
372	VCI	6229	-385
373	VCI	6269	-385
374	VCI	6309	-385
375	DUMMY	6349	-385
376	C12B	6389	-385
377	C12B	6429	-385
378	C12B	6469	-385
379	C12B	6509	-385
380	C12B	6549	-385
381	C12B	6589	-385
382	C12B	6629	-385
383	C12B	6669	-385
384	C12A	6709	-385
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386	C12A	6789	-385
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394	C21B	7109	-385
395	C21B	7149	-385
396	C21B	7189	-385
397	C21B	7229	-385
398	C21B	7269	-385
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401	C21B	7389	-385
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405	C21A	7549	-385
406	C21A	7589	-385
407	C21A	7629	-385
408	C21A	7669	-385
409	C21A	7709	-385
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411	C21A	7789	-385
412	C21A	7829	-385
413	C21A	7869	-385
414	C21A	7909	-385
415	C21A	7949	-385
416	C22B	7989	-385
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418	C22B	8069	-385
419	C22B	8109	-385
420	C22B	8149	-385

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426	C22B	8389	-385
427	C22B	8429	-385
428	C22A	8469	-385
429	C22A	8509	-385
430	C22A	8549	-385
431	C22A	8589	-385
432	C22A	8629	-385
433	C22A	8669	-385
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435	C22A	8749	-385
436	C22A	8789	-385
437	C22A	8829	-385
438	C22A	8869	-385
439	C22A	8909	-385
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441	DUMMYR4	8989	-385
442	PADB0	9029	-385
443	PADB2	9069	-385
444	PADA2	9109	-385
445	DUMMY	9149	-385
446	DUMMY	9189	-385
447	DUMMY	9223	-238
448	DUMMY	9101	-222
449	DUMMY	9223	-206
450	G480	9101	-190
451	G478	9223	-174
452	G476	9101	-158
453	G474	9223	-142
454	G472	9101	-126
455	G470	9223	-110
456	G468	9101	-94
457	G466	9223	-78
458	G464	9101	-62
459	G462	9223	-46
460	G460	9101	-30
461	G458	9223	-14
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463	G454	9223	18
464	G452	9101	34
465	G450	9223	50
466	G448	9101	66
467	G446	9223	82
468	G444	9101	98
469	G442	9223	114
470	G440	9101	130
471	G438	9223	146
472	G436	9101	162
473	G434	9223	178
474	DUMMY	9101	194
475	DUMMY	9223	210
476	DUMMY	9101	226
477	DUMMY	9223	242
478	DUMMY	9007	393
479	DUMMY	8991	271
480	PADA3	8975	393

Himax Confidential
Himax Confidential

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483	G430	8927	271
484	G428	8911	393
485	G426	8895	271
486	G424	8879	393
487	G422	8863	271
488	G420	8847	393
489	G418	8831	271
490	G416	8815	393
491	G414	8799	271
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493	G410	8767	271
494	G408	8751	393
495	G406	8735	271
496	G404	8719	393
497	G402	8703	271
498	G400	8687	393
499	G398	8671	271
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501	G394	8639	271
502	G392	8623	393
503	G390	8607	271
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509	G378	8511	271
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511	G374	8479	271
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513	G370	8447	271
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517	G362	8383	271
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519	G358	8351	271
520	G356	8335	393
521	G354	8319	271
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525	G346	8255	271
526	G344	8239	393
527	G342	8223	271
528	G340	8207	393
529	G338	8191	271
530	G336	8175	393
531	G334	8159	271
532	G332	8143	393
533	G330	8127	271
534	G328	8111	393
535	G326	8095	271
536	G324	8079	393
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538	G320	8047	393
539	G318	8031	271
540	G316	8015	393

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543	G310	7967	271
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546	G304	7919	393
547	G302	7903	271
548	G300	7887	393
549	G298	7871	271
550	G296	7855	393
551	G294	7839	271
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553	G290	7807	271
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557	G282	7743	271
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559	G278	7711	271
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561	G274	7679	271
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563	G270	7647	271
564	G268	7631	393
565	G266	7615	271
566	G264	7599	393
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569	G258	7551	271
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571	G254	7519	271
572	G252	7503	393
573	G250	7487	271
574	G248	7471	393
575	G246	7455	271
576	G244	7439	393
577	G242	7423	271
578	G240	7407	393
579	G238	7391	271
580	G236	7375	393
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582	G232	7343	393
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597	G202	7103	271
598	G200	7087	393
599	G198	7071	271
600	G196	7055	393

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613	G170	6847	271
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621	G154	6719	271
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627	G142	6623	271
628	G140	6607	393
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643	G110	6367	271
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655	G86	6175	271
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657	G82	6143	271
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659	G78	6111	271
660	G76	6095	393

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668	G60	5967	393
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671	G54	5919	271
672	G52	5903	393
673	G50	5887	271
674	G48	5871	393
675	G46	5855	271
676	G44	5839	393
677	G42	5823	271
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679	G38	5791	271
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681	G34	5759	271
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695	G6	5535	271
696	G4	5519	393
697	G2	5503	271
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699	DUMMY	5471	271
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701	DUMMY	5441	271
702	S720	5427	393
703	S719	5413	271
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717	S705	5217	271
718	S704	5203	393
719	S703	5189	271
720	S702	5175	393

Himax Confidential
Himax Confidential

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724	S698	5119	393
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729	S693	5049	271
730	S692	5035	393
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732	S690	5007	393
733	S689	4993	271
734	S688	4979	393
735	S687	4965	271
736	S686	4951	393
737	S685	4937	271
738	S684	4923	393
739	S683	4909	271
740	S682	4895	393
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743	S679	4853	271
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768	S654	4503	393
769	S653	4489	271
770	S652	4475	393
771	S651	4461	271
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779	S643	4349	271
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787	S635	4237	271
788	S634	4223	393
789	S633	4209	271
790	S632	4195	393
791	S631	4181	271
792	S630	4167	393
793	S629	4153	271
794	S628	4139	393
795	S627	4125	271
796	S626	4111	393
797	S625	4097	271
798	S624	4083	393
799	S623	4069	271
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801	S621	4041	271
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803	S619	4013	271
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806	S616	3971	393
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813	S609	3873	271
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816	S606	3831	393
817	S605	3817	271
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835	S587	3565	271
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839	S583	3509	271
840	S582	3495	393

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843	S579	3453	271
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846	S576	3411	393
847	S575	3397	271
848	S574	3383	393
849	S573	3369	271
850	S572	3355	393
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853	S569	3313	271
854	S568	3299	393
855	S567	3285	271
856	S566	3271	393
857	S565	3257	271
858	S564	3243	393
859	S563	3229	271
860	S562	3215	393
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862	S560	3187	393
863	S559	3173	271
864	S558	3159	393
865	S557	3145	271
866	S556	3131	393
867	S555	3117	271
868	S554	3103	393
869	S553	3089	271
870	S552	3075	393
871	S551	3061	271
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873	S549	3033	271
874	S548	3019	393
875	S547	3005	271
876	S546	2991	393
877	S545	2977	271
878	S544	2963	393
879	S543	2949	271
880	S542	2935	393
881	S541	2921	271
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887	S535	2837	271
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889	S533	2809	271
890	S532	2795	393
891	S531	2781	271
892	S530	2767	393
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895	S527	2725	271
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899	S523	2669	271
900	S522	2655	393

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905	S517	2585	271
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909	S513	2529	271
910	S512	2515	393
911	S511	2501	271
912	S510	2487	393
913	S509	2473	271
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916	S506	2431	393
917	S505	2417	271
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923	S499	2333	271
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925	S497	2305	271
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931	S491	2221	271
932	S490	2207	393
933	S489	2193	271
934	S488	2179	393
935	S487	2165	271
936	S486	2151	393
937	S485	2137	271
938	S484	2123	393
939	S483	2109	271
940	S482	2095	393
941	S481	2081	271
942	S480	2067	393
943	S479	2053	271
944	S478	2039	393
945	S477	2025	271
946	S476	2011	393
947	S475	1997	271
948	S474	1983	393
949	S473	1969	271
950	S472	1955	393
951	S471	1941	271
952	S470	1927	393
953	S469	1913	271
954	S468	1899	393
955	S467	1885	271
956	S466	1871	393
957	S465	1857	271
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959	S463	1829	271
960	S462	1815	393

Himax Confidential
Himax Confidential

No.	Name	X	Y
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968	S454	1703	393
969	S453	1689	271
970	S452	1675	393
971	S451	1661	271
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973	S449	1633	271
974	S448	1619	393
975	S447	1605	271
976	S446	1591	393
977	S445	1577	271
978	S444	1563	393
979	S443	1549	271
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981	S441	1521	271
982	S440	1507	393
983	S439	1493	271
984	S438	1479	393
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986	S436	1451	393
987	S435	1437	271
988	S434	1423	393
989	S433	1409	271
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993	S429	1353	271
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995	S427	1325	271
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997	S425	1297	271
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1001	S421	1241	271
1002	S420	1227	393
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1009	S413	1129	271
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1017	S405	1017	271
1018	S404	1003	393
1019	S403	989	271
1020	S402	975	393

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1028	S394	863	393
1029	S393	849	271
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1033	S389	793	271
1034	S388	779	393
1035	S387	765	271
1036	S386	751	393
1037	S385	737	271
1038	S384	723	393
1039	S383	709	271
1040	S382	695	393
1041	S381	681	271
1042	S380	667	393
1043	S379	653	271
1044	S378	639	393
1045	S377	625	271
1046	S376	611	393
1047	S375	597	271
1048	S374	583	393
1049	S373	569	271
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1051	S371	541	271
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1053	S369	513	271
1054	S368	499	393
1055	S367	485	271
1056	S366	471	393
1057	S365	457	271
1058	S364	443	393
1059	S363	429	271
1060	S362	415	393
1061	S361	401	271
1062	DUMMY	387	393
1063	DUMMY	373	271
1064	DUMMY	359	393
1065	DUMMY	331	393
1066	DUMMY	303	393
1067	DUMMY	275	393
1068	DUMMY	247	393
1069	DUMMY	219	393
1070	DUMMY	191	393
1071	DUMMY	163	393
1072	DUMMY	135	393
1073	DUMMY	107	393
1074	DUMMY	79	393
1075	DUMMY	51	393
1076	DUMMY	23	393
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1078	DUMMY	-51	393
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No.	Name	X	Y
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1082	DUMMY	-163	393
1083	DUMMY	-191	393
1084	DUMMY	-219	393
1085	DUMMY	-247	393
1086	DUMMY	-275	393
1087	DUMMY	-303	393
1088	DUMMY	-331	393
1089	DUMMY	-359	393
1090	DUMMY	-373	271
1091	DUMMY	-387	393
1092	S360	-401	271
1093	S359	-415	393
1094	S358	-429	271
1095	S357	-443	393
1096	S356	-457	271
1097	S355	-471	393
1098	S354	-485	271
1099	S353	-499	393
1100	S352	-513	271
1101	S351	-527	393
1102	S350	-541	271
1103	S349	-555	393
1104	S348	-569	271
1105	S347	-583	393
1106	S346	-597	271
1107	S345	-611	393
1108	S344	-625	271
1109	S343	-639	393
1110	S342	-653	271
1111	S341	-667	393
1112	S340	-681	271
1113	S339	-695	393
1114	S338	-709	271
1115	S337	-723	393
1116	S336	-737	271
1117	S335	-751	393
1118	S334	-765	271
1119	S333	-779	393
1120	S332	-793	271
1121	S331	-807	393
1122	S330	-821	271
1123	S329	-835	393
1124	S328	-849	271
1125	S327	-863	393
1126	S326	-877	271
1127	S325	-891	393
1128	S324	-905	271
1129	S323	-919	393
1130	S322	-933	271
1131	S321	-947	393
1132	S320	-961	271
1133	S319	-975	393
1134	S318	-989	271
1135	S317	-1003	393
1136	S316	-1017	271
1137	S315	-1031	393
1138	S314	-1045	271
1139	S313	-1059	393
1140	S312	-1073	271

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1142	S310	-1101	271
1143	S309	-1115	393
1144	S308	-1129	271
1145	S307	-1143	393
1146	S306	-1157	271
1147	S305	-1171	393
1148	S304	-1185	271
1149	S303	-1199	393
1150	S302	-1213	271
1151	S301	-1227	393
1152	S300	-1241	271
1153	S299	-1255	393
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1155	S297	-1283	393
1156	S296	-1297	271
1157	S295	-1311	393
1158	S294	-1325	271
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1160	S292	-1353	271
1161	S291	-1367	393
1162	S290	-1381	271
1163	S289	-1395	393
1164	S288	-1409	271
1165	S287	-1423	393
1166	S286	-1437	271
1167	S285	-1451	393
1168	S284	-1465	271
1169	S283	-1479	393
1170	S282	-1493	271
1171	S281	-1507	393
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1173	S279	-1535	393
1174	S278	-1549	271
1175	S277	-1563	393
1176	S276	-1577	271
1177	S275	-1591	393
1178	S274	-1605	271
1179	S273	-1619	393
1180	S272	-1633	271
1181	S271	-1647	393
1182	S270	-1661	271
1183	S269	-1675	393
1184	S268	-1689	271
1185	S267	-1703	393
1186	S266	-1717	271
1187	S265	-1731	393
1188	S264	-1745	271
1189	S263	-1759	393
1190	S262	-1773	271
1191	S261	-1787	393
1192	S260	-1801	271
1193	S259	-1815	393
1194	S258	-1829	271
1195	S257	-1843	393
1196	S256	-1857	271
1197	S255	-1871	393
1198	S254	-1885	271
1199	S253	-1899	393
1200	S252	-1913	271

Himax Confidential
FOR CUSTOMER USE ONLY

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1201	S251	-1927	393
1202	S250	-1941	271
1203	S249	-1955	393
1204	S248	-1969	271
1205	S247	-1983	393
1206	S246	-1997	271
1207	S245	-2011	393
1208	S244	-2025	271
1209	S243	-2039	393
1210	S242	-2053	271
1211	S241	-2067	393
1212	S240	-2081	271
1213	S239	-2095	393
1214	S238	-2109	271
1215	S237	-2123	393
1216	S236	-2137	271
1217	S235	-2151	393
1218	S234	-2165	271
1219	S233	-2179	393
1220	S232	-2193	271
1221	S231	-2207	393
1222	S230	-2221	271
1223	S229	-2235	393
1224	S228	-2249	271
1225	S227	-2263	393
1226	S226	-2277	271
1227	S225	-2291	393
1228	S224	-2305	271
1229	S223	-2319	393
1230	S222	-2333	271
1231	S221	-2347	393
1232	S220	-2361	271
1233	S219	-2375	393
1234	S218	-2389	271
1235	S217	-2403	393
1236	S216	-2417	271
1237	S215	-2431	393
1238	S214	-2445	271
1239	S213	-2459	393
1240	S212	-2473	271
1241	S211	-2487	393
1242	S210	-2501	271
1243	S209	-2515	393
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1255	S197	-2683	393
1256	S196	-2697	271
1257	S195	-2711	393
1258	S194	-2725	271
1259	S193	-2739	393
1260	S192	-2753	271

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1262	S190	-2781	271
1263	S189	-2795	393
1264	S188	-2809	271
1265	S187	-2823	393
1266	S186	-2837	271
1267	S185	-2851	393
1268	S184	-2865	271
1269	S183	-2879	393
1270	S182	-2893	271
1271	S181	-2907	393
1272	S180	-2921	271
1273	S179	-2935	393
1274	S178	-2949	271
1275	S177	-2963	393
1276	S176	-2977	271
1277	S175	-2991	393
1278	S174	-3005	271
1279	S173	-3019	393
1280	S172	-3033	271
1281	S171	-3047	393
1282	S170	-3061	271
1283	S169	-3075	393
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1286	S166	-3117	271
1287	S165	-3131	393
1288	S164	-3145	271
1289	S163	-3159	393
1290	S162	-3173	271
1291	S161	-3187	393
1292	S160	-3201	271
1293	S159	-3215	393
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1297	S155	-3271	393
1298	S154	-3285	271
1299	S153	-3299	393
1300	S152	-3313	271
1301	S151	-3327	393
1302	S150	-3341	271
1303	S149	-3355	393
1304	S148	-3369	271
1305	S147	-3383	393
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1318	S134	-3565	271
1319	S133	-3579	393
1320	S132	-3593	271

No.	Name	X	Y
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1337	S115	-3831	393
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1340	S112	-3873	271
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1352	S100	-4041	271
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1357	S95	-4111	393
1358	S94	-4125	271
1359	S93	-4139	393
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1361	S91	-4167	393
1362	S90	-4181	271
1363	S89	-4195	393
1364	S88	-4209	271
1365	S87	-4223	393
1366	S86	-4237	271
1367	S85	-4251	393
1368	S84	-4265	271
1369	S83	-4279	393
1370	S82	-4293	271
1371	S81	-4307	393
1372	S80	-4321	271
1373	S79	-4335	393
1374	S78	-4349	271
1375	S77	-4363	393
1376	S76	-4377	271
1377	S75	-4391	393
1378	S74	-4405	271
1379	S73	-4419	393
1380	S72	-4433	271

No.	Name	X	Y
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1384	S68	-4489	271
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1396	S56	-4657	271
1397	S55	-4671	393
1398	S54	-4685	271
1399	S53	-4699	393
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1429	S23	-5119	393
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1431	S21	-5147	393
1432	S20	-5161	271
1433	S19	-5175	393
1434	S18	-5189	271
1435	S17	-5203	393
1436	S16	-5217	271
1437	S15	-5231	393
1438	S14	-5245	271
1439	S13	-5259	393
1440	S12	-5273	271

Himax Confidential
Himax Confidential

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1442	S10	-5301	271
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1445	S7	-5343	393
1446	S6	-5357	271
1447	S5	-5371	393
1448	S4	-5385	271
1449	S3	-5399	393
1450	S2	-5413	271
1451	S1	-5427	393
1452	DUMMY	-5441	271
1453	DUMMY	-5455	393
1454	DUMMY	-5471	271
1455	DUMMY	-5487	393
1456	G1	-5503	271
1457	G3	-5519	393
1458	G5	-5535	271
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1464	G17	-5631	271
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1471	G31	-5743	393
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1497	G83	-6159	393
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1670	G429	-8927	271
1671	G431	-8943	393
1672	PADB4	-8959	271
1673	PADA4	-8975	393
1674	DUMMY	-8991	271
1675	DUMMY	-9007	393
1676	DUMMY	-9223	242
1677	DUMMY	-9101	226
1678	DUMMY	-9223	210
1679	DUMMY	-9101	194
1680	G433	-9223	178

Himax Confidential
Do Not Copy

No.	Name	X	Y
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1683	G439	-9101	130
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1687	G447	-9101	66
1688	G449	-9223	50
1689	G451	-9101	34
1690	G453	-9223	18
1691	G455	-9101	2
1692	G457	-9223	-14
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1694	G461	-9223	-46
1695	G463	-9101	-62
1696	G465	-9223	-78
1697	G467	-9101	-94
1698	G469	-9223	-110
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1700	G473	-9223	-142
1701	G475	-9101	-158
1702	G477	-9223	-174
1703	G479	-9101	-190
1704	DUMMY	-9223	-206
1705	DUMMY	-9101	-222
1706	DUMMY	-9223	-238

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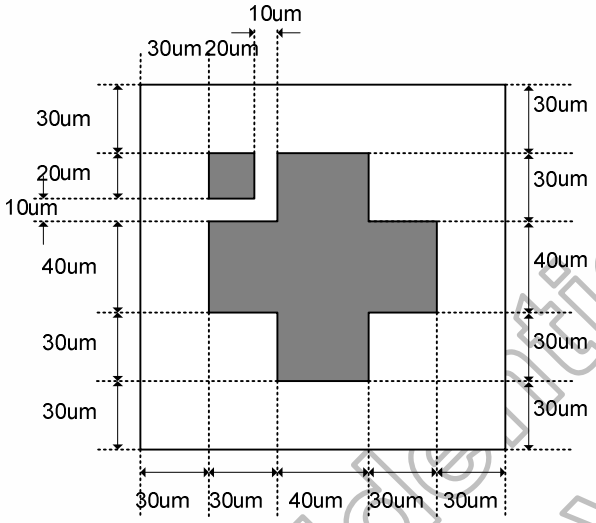
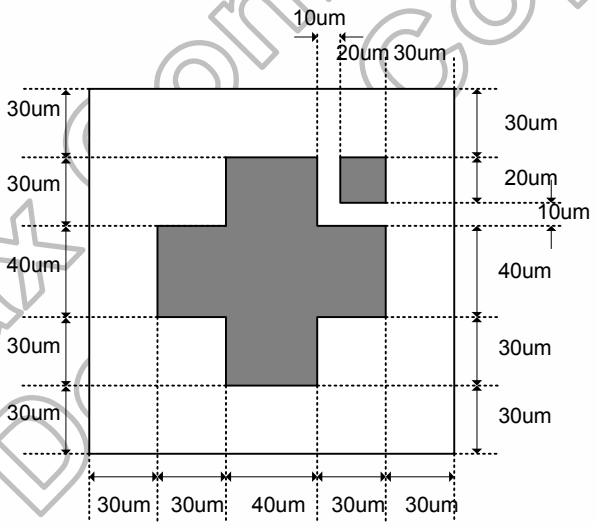
4.4 Alignment mark



A1 (-9200,+370)



A2 (+9200,+370)

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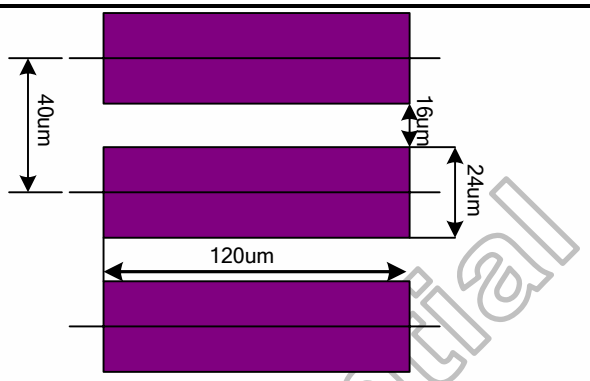
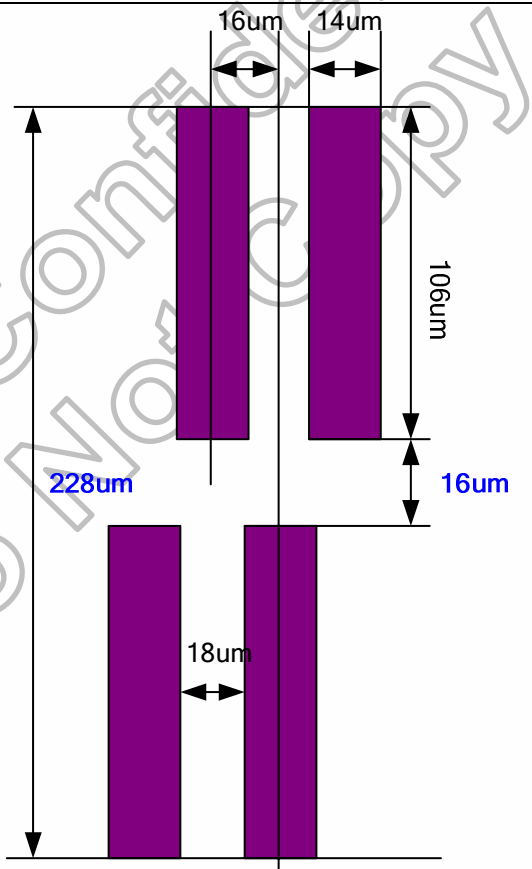
4.5 Bump size

Input PAD	 NO.1~NO.446
Output PAD	 NO.447~NO.477

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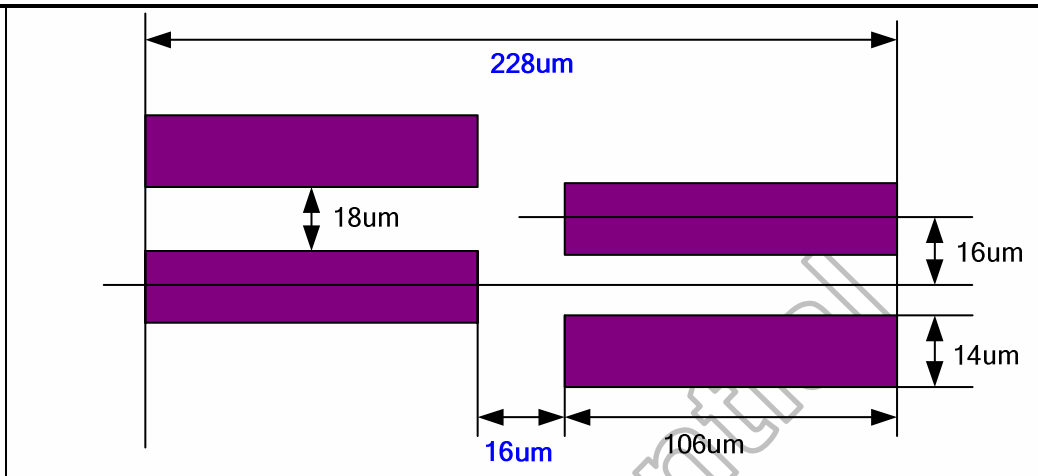

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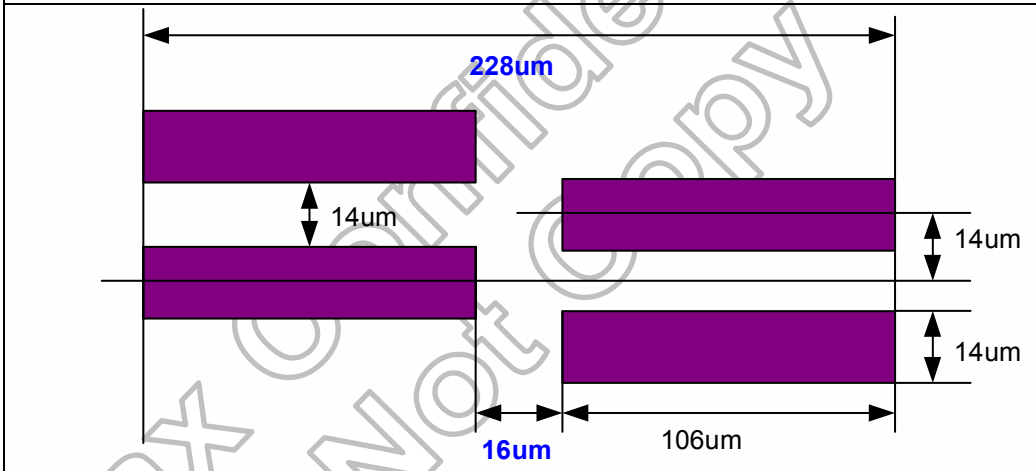

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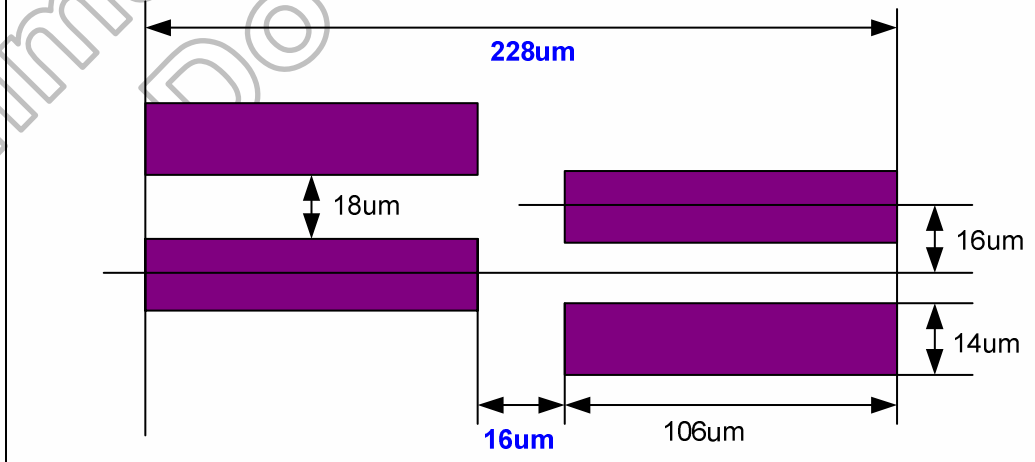

NO.1454~NO.1675

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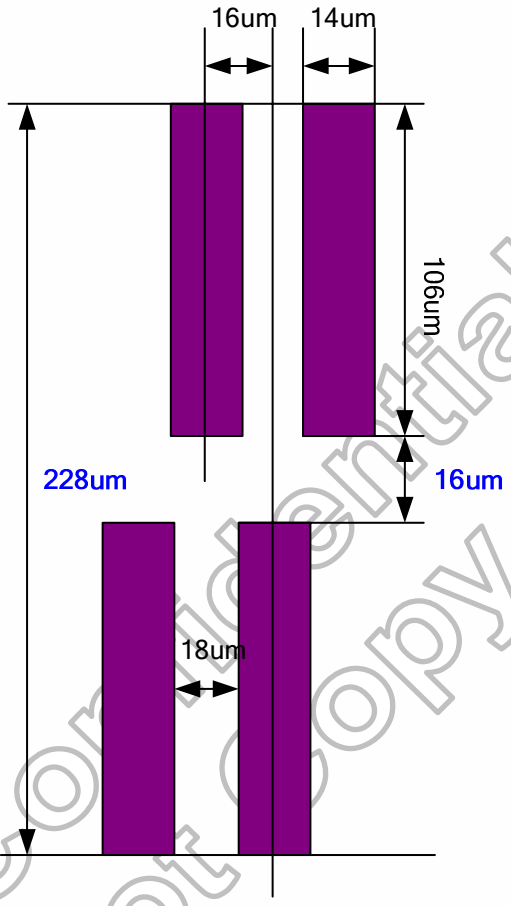

NO.1676~NO.1706

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5. Function Description

5.1 Interface control mode

The HX8352-A supports four-type interface mode: Command-Parameter interface mode, Register-Content interface mode, RGB interface mode. Command-Parameter interface mode, Register-Content interface mode are selected by the external pins IFSEL0, BS2-0 setting as shown in Table5.1. There are two-type chip access formats in HX8352-A. One is register command for chip internal operation. The other is display data for chip display.

IFSEL0	BS2-0	Register Data	Display Data
0	000, 001, 010, 011, 100, 101, 110	Command-Parameter interface (MPU interface)	GRAM
0	111	Command-Parameter interface (SPI + RGB interface)	Normal: RGB interface
1	000, 001, 010, 011, 100	Register-Content interface (MPU interface)	GRAM
1	11x	Register-Content interface (SPI + RGB interface)	Normal: RGB interface

Table 5. 1 Interface Mode Selection

There are two-type register groups in HX8352-A. One is accessed only via Command-Parameter interface. The other is accessed only via Register-Content interface.

This manual description focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode; please refer to the HX8352-A(N) datasheet for detail.

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5.1.1 Register-content interface mode

The register-content interface circuit in HX8352-A supports 18-/16-/8-bit bus width parallel bus system interface for I80 series and M68 series CPU, and serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8352-A become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS(2-0) setting. For selecting the input bus format, please refer to Table5.2 and Table5.3.

In Register-Content interface, it includes an Index Register (IR) be stored index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

P68	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 5. 2 MPU selection in Register-content Interface Circuit

BS2	BS1	BS0	Interface	Transferring Method of RAM data	Transferring Method of Command
0	0	0	16-bit system interface	16-bit collective	8-bit collective
0	0	1		16-bit + 2 bit	
0	1	0	18-bit system interface	18-bit collective	
0	1	1	8-bit system interface	8-bit + 8-bit + 8-bit	
1	0	0		8-bit + 8-bit	
1	1	x	Serial bus transfer interface	16 or 24-bit serial	8-bit serial

Table 5. 3 Interface Selection in Register-content Interface Mode

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5.1.2 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80/M68 series parallel bus interface are listed in Table 5.2.

Operations	NRD_E	NWR_RNW	DNC_SCL
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5. 4 Data Pin Function for I80 Series CPU

Operations	NRD_E	NWR_RNW	DNC_SCL
Writes Indexes into IR	1	0	0
Reads internal status	1	1	0
Writes command into register or data into GRAM	1	0	1
Reads command from register or data from GRAM	1	1	1

Table 5. 5 Data Pin Function for M68 Series CPU

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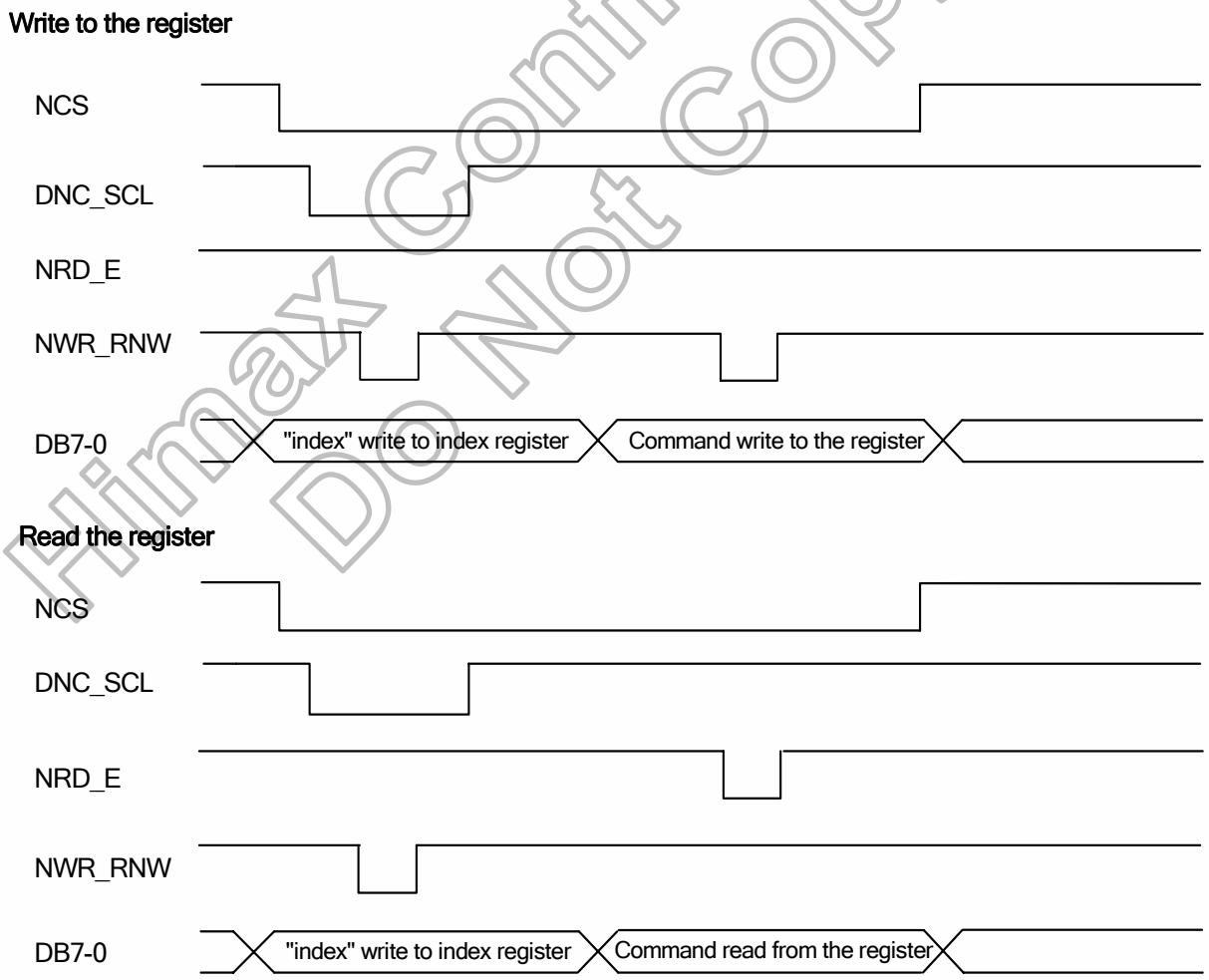

Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

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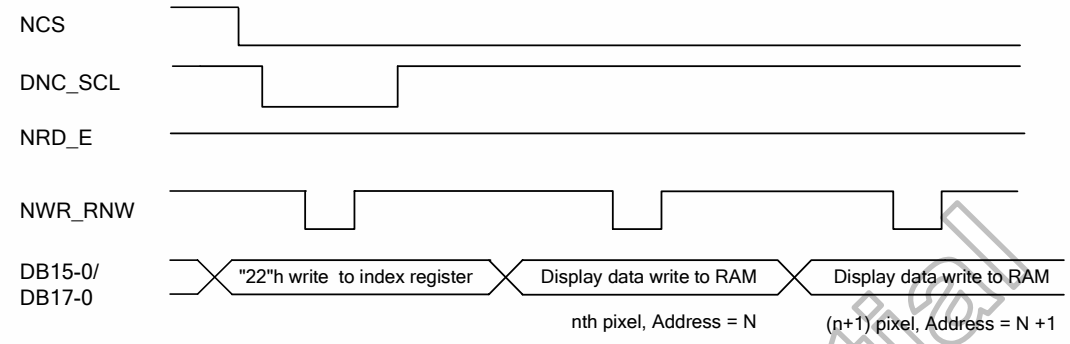
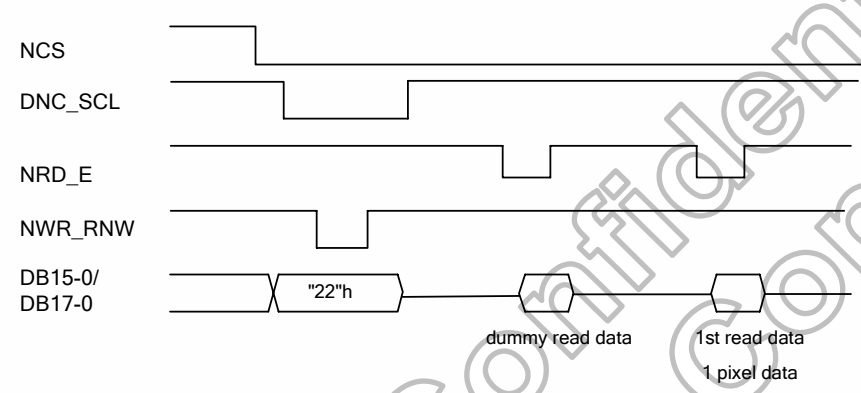
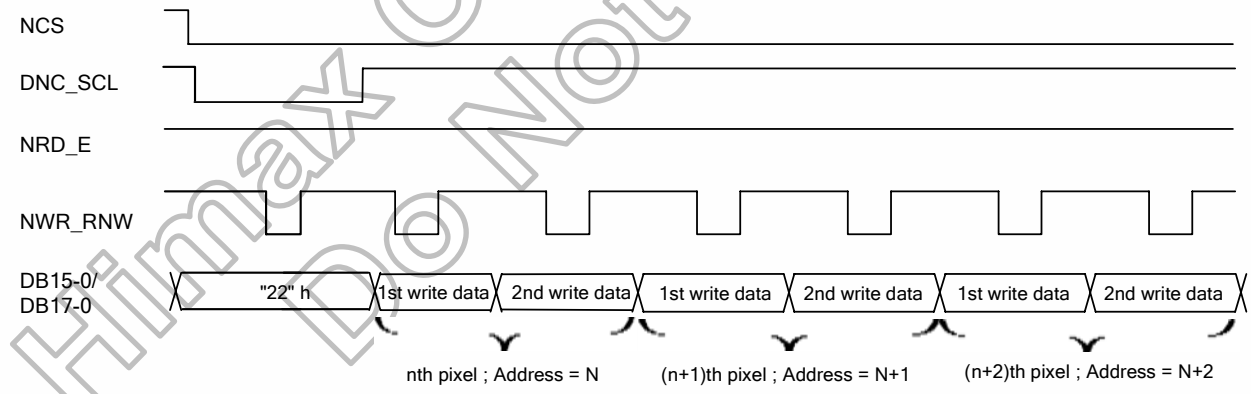
Write to the graphic RAM (16-bit 65K Color / 18-bit bit 262K Color)



Read the graphic RAM (16-bit 65K Color / 18-bit bit 262K Color)



Write to the graphic RAM (16+2-bit 262K Color / 8+8-bit 65K Color)



Read the graphic RAM (16+2 bit 262K Color / 8+8-bit 65K Color)

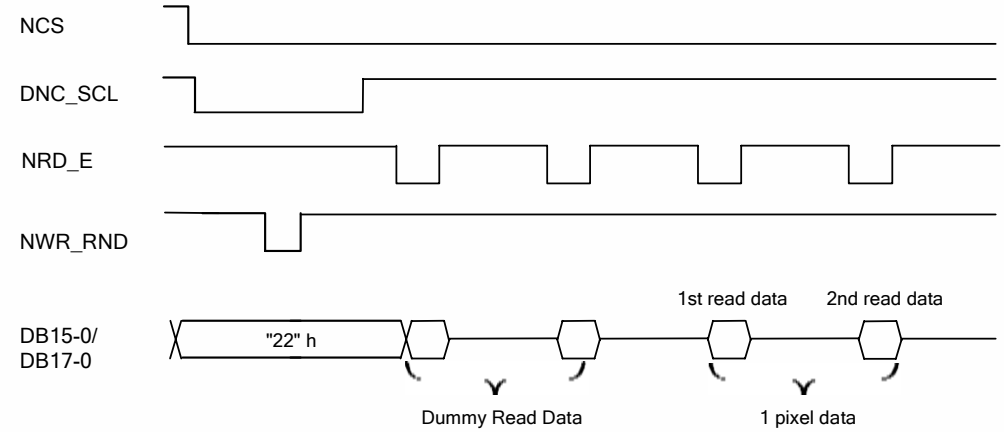


Figure 5. 2 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for I80 Series MPU)

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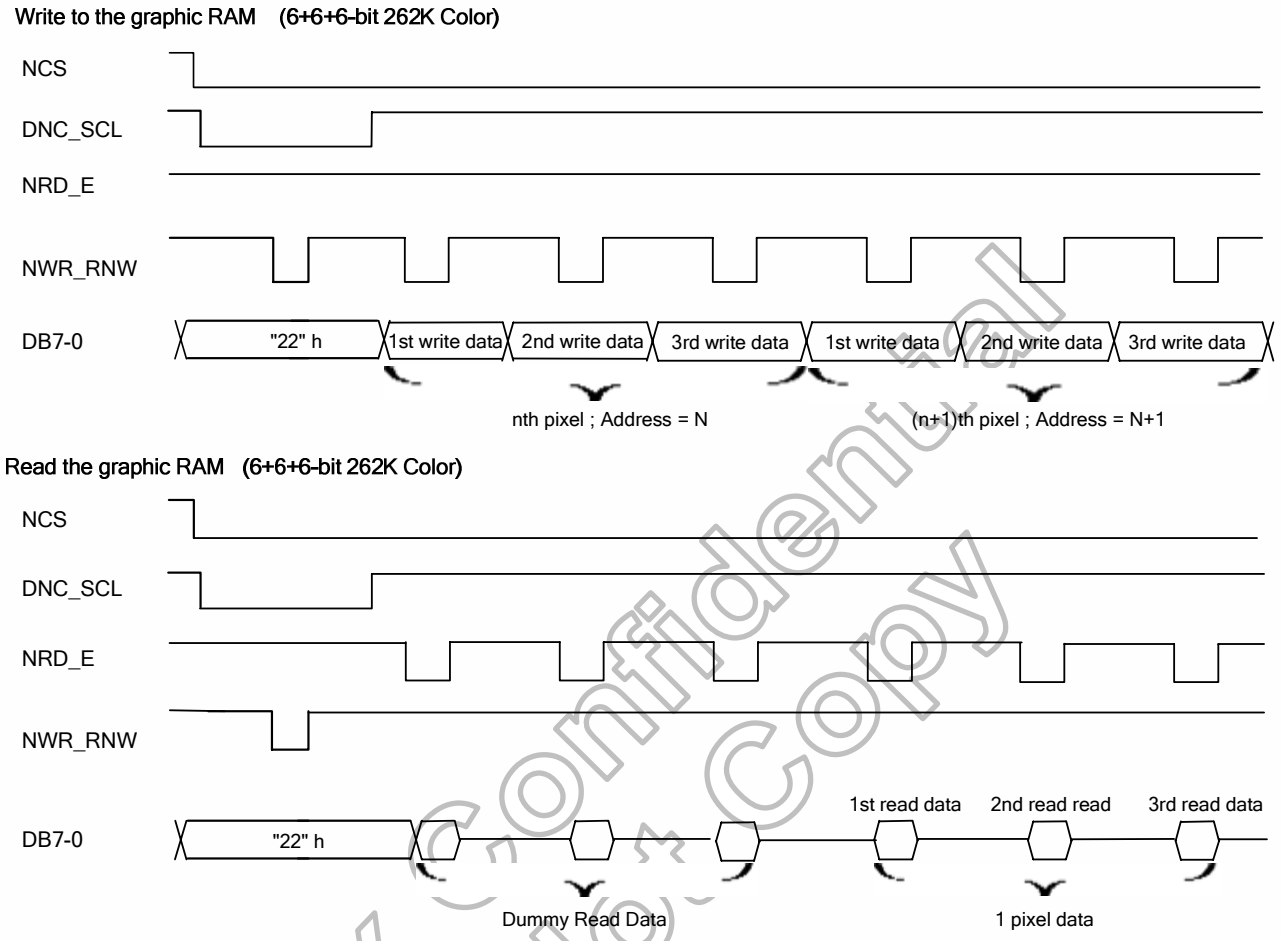

Figure 5. 3 GRAM Read/Write Timing in 8-Bit Parallel Bus System Interface (for I80 Series MPU)

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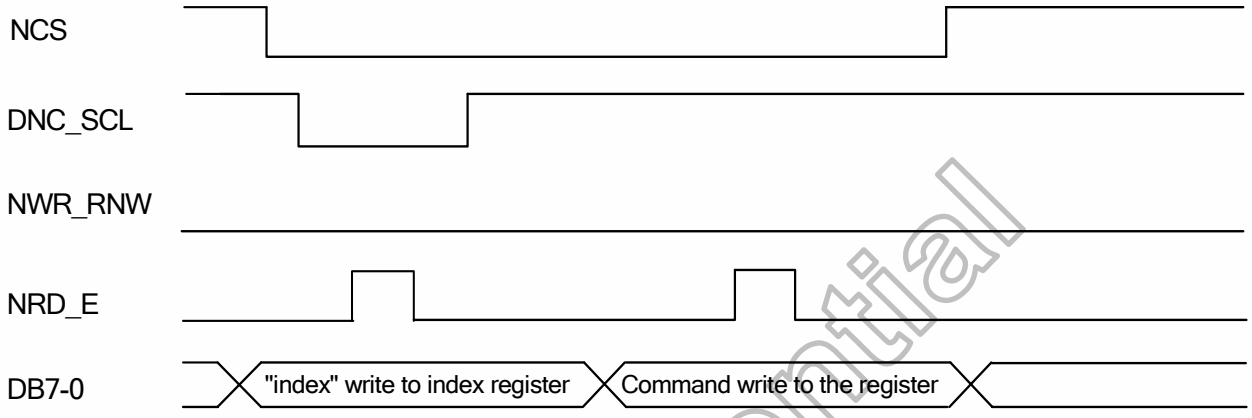
Write to the register



Read the register

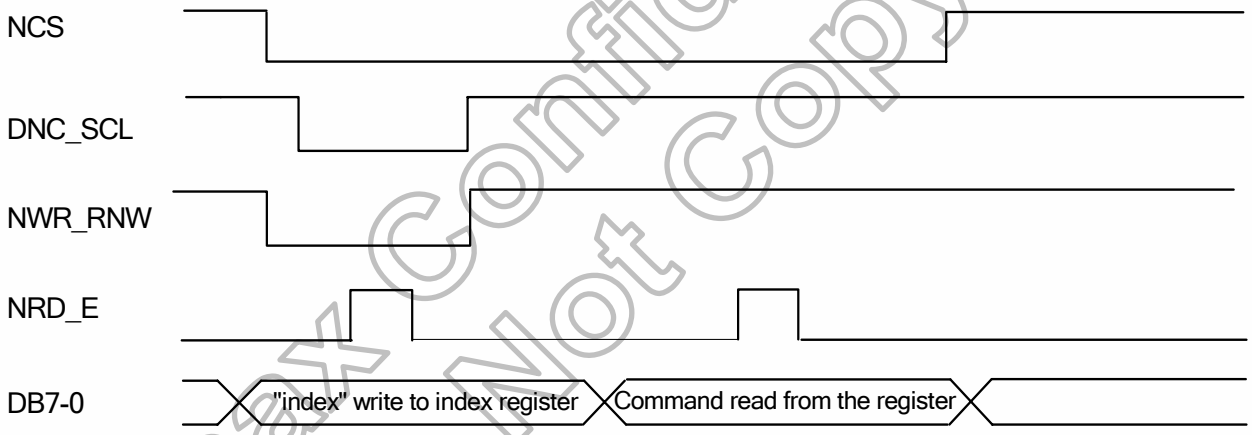


Figure 5. 4 Register Read/Write Timing in Parallel Bus System Interface (for M68 Series MPU)

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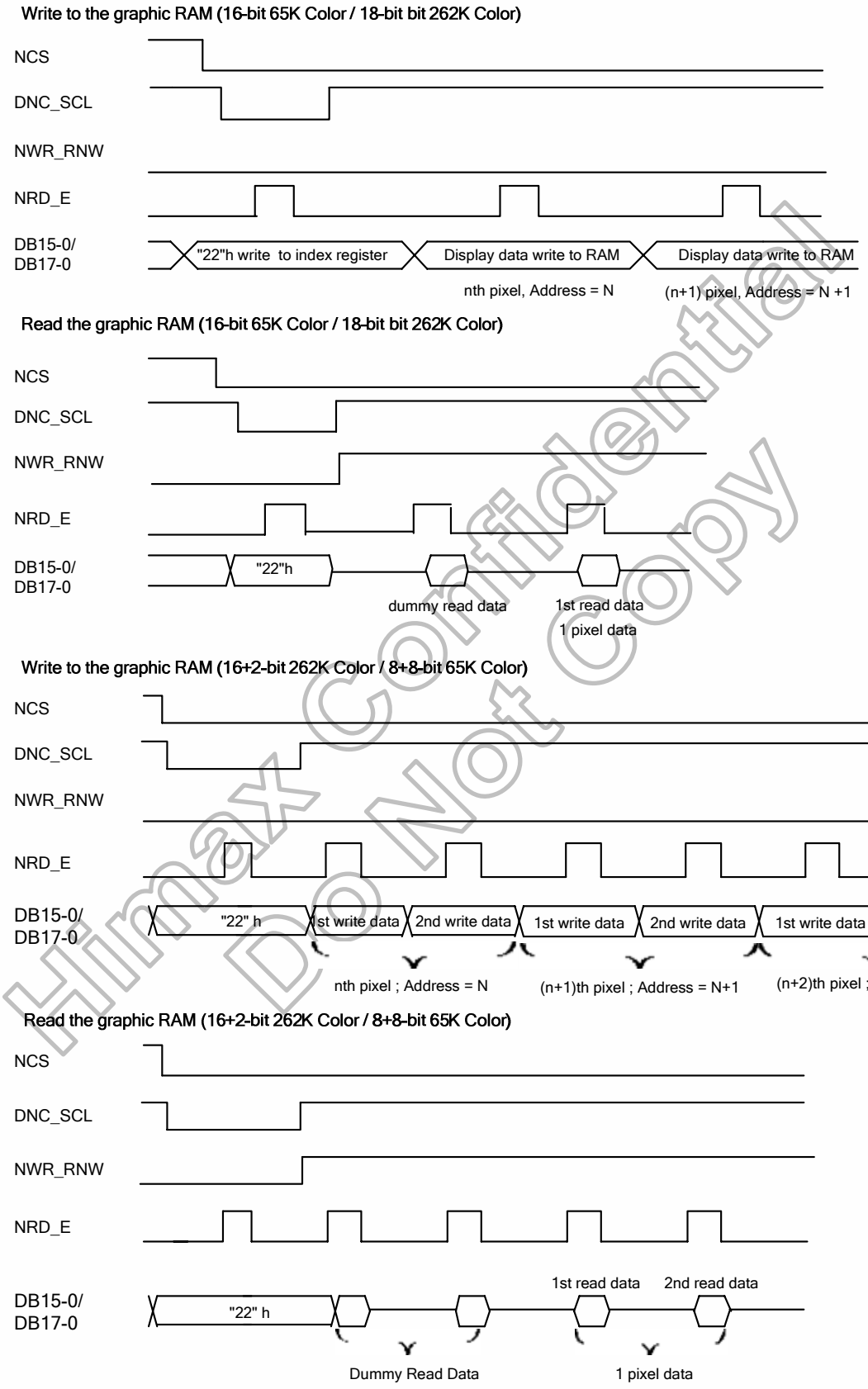

Figure 5. 5 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for M68 Series MPU)

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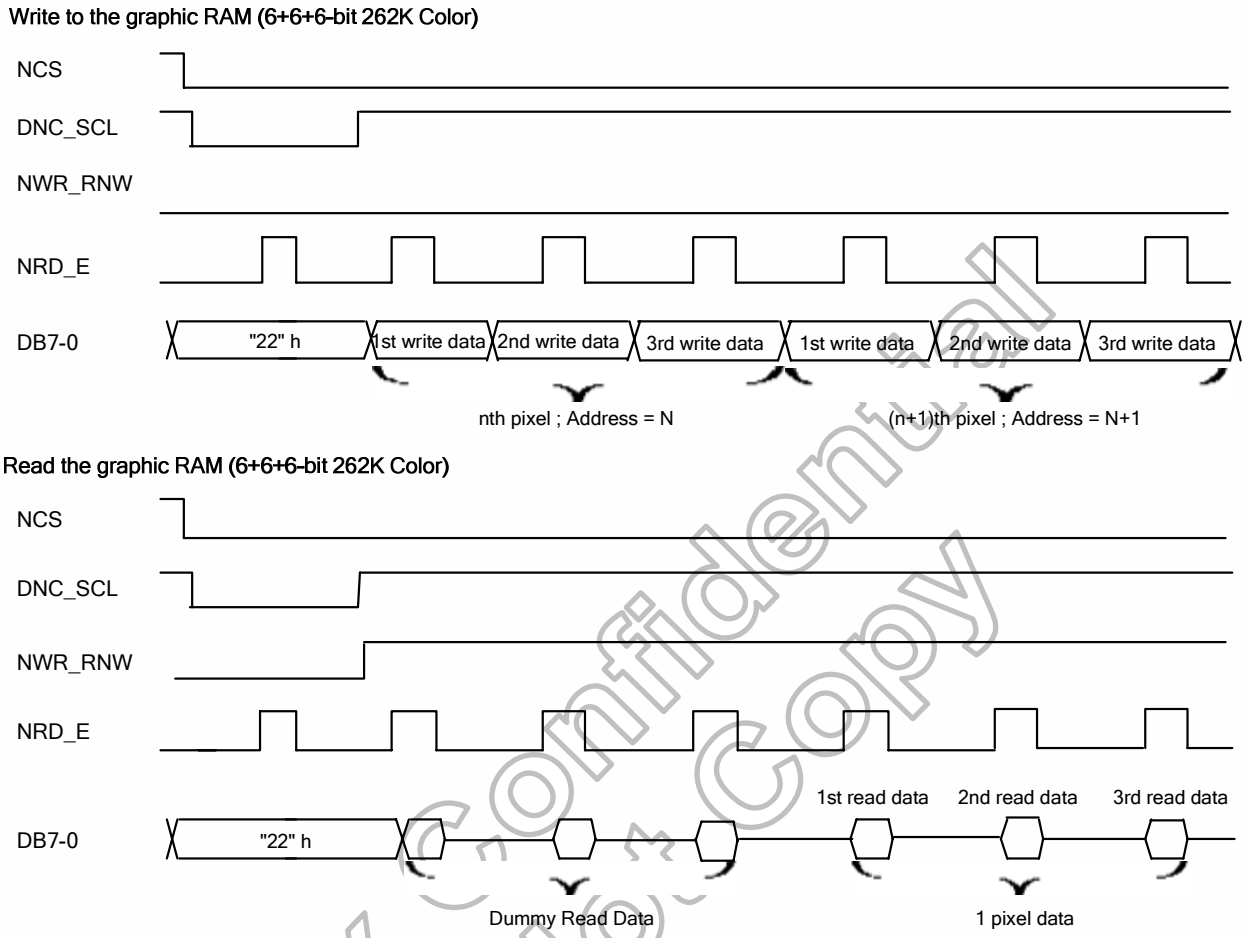

Figure 5. 6 GRAM Read/Write Timing in 8-bit Parallel Bus System Interface (for M68 Series MPU)

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18-bit Parallel bus system interface

The I80-system 18-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0010”. And the M68-system 18-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, and BS0” pins to “1010”. Figure 5.7 is the example of interface with I80/M68 microcomputer system interface.

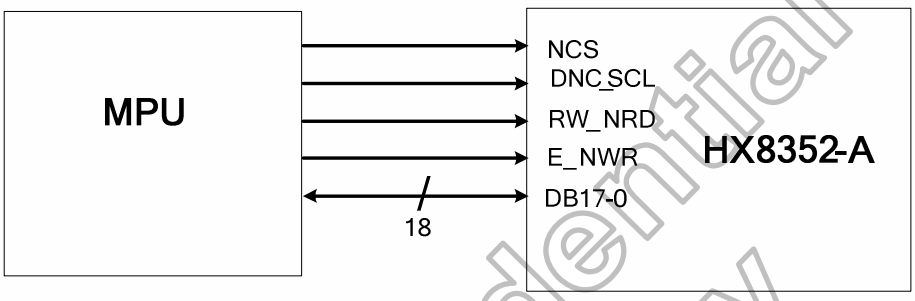

Figure 5. 7 Example of I80- / M68- System 16-Bit Parallel Bus Interface

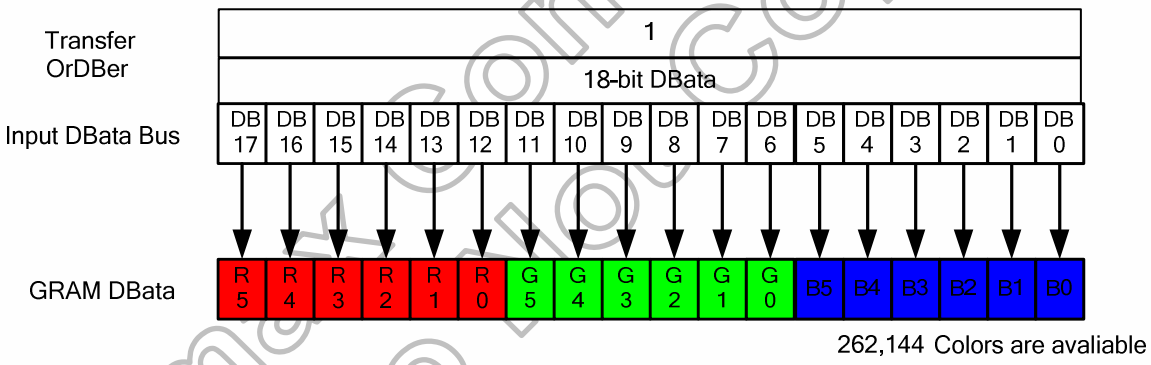

Figure 5. 8 Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface (“BS2, BS1, BS0”=”010”)

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16-bit Parallel bus system interface

The I80-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0000”, “0001”, “0100”. And the M68-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1000”, “1001”, “1100”. Figure 5.9 is the example of interface with I80/M68 microcomputer system interface.

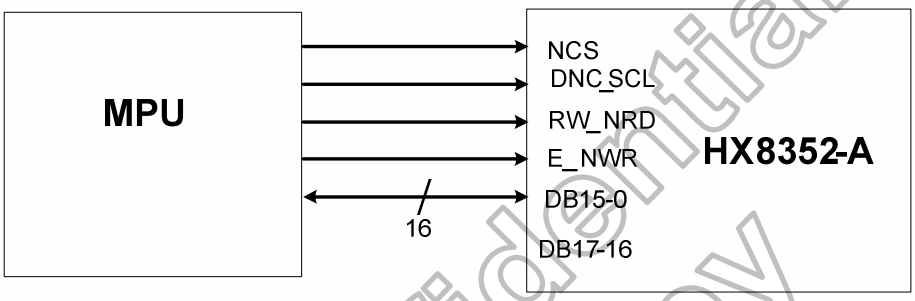

Figure 5. 9 Example of I80- / M68- System 16-bit Parallel Bus Interface

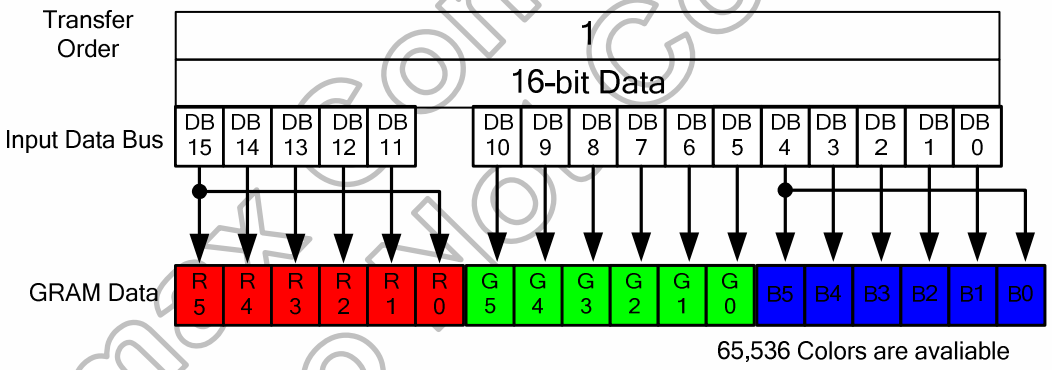

Figure 5. 10 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input (“BS2, BS1, BS0”=”000”)

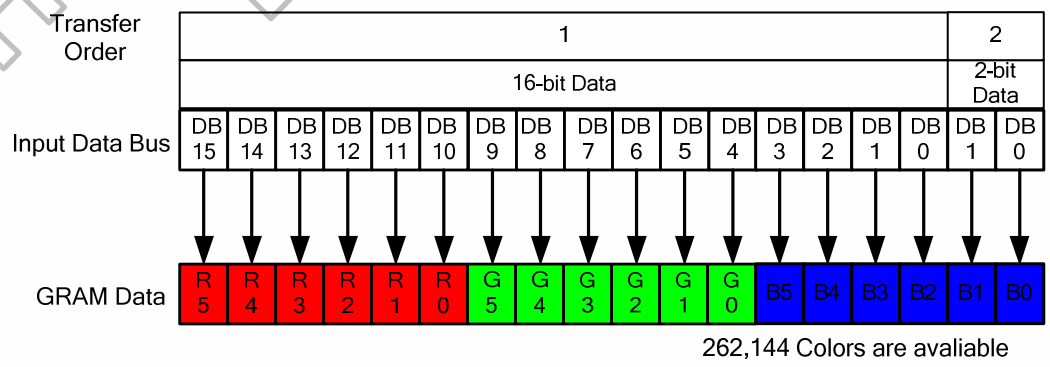

Figure 5. 11 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input (“BS2, BS1, BS0”=”001”)

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8-bit Parallel bus system interface

The I80-system 8-bit parallel bus interface in register-content interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0011” or “0100”. And the M68-system 8-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1011” or “0100”. Figure 5.13~16 are the example of interface with I80/M68 microcomputer system interface.

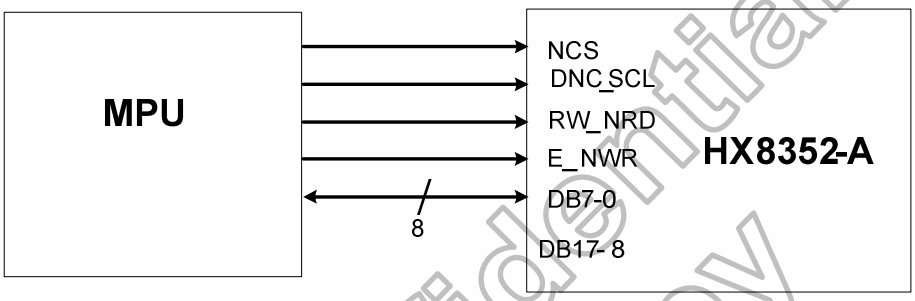

Figure 5. 12 Example of I80- / M68- System 8-Bit Parallel Bus Interface

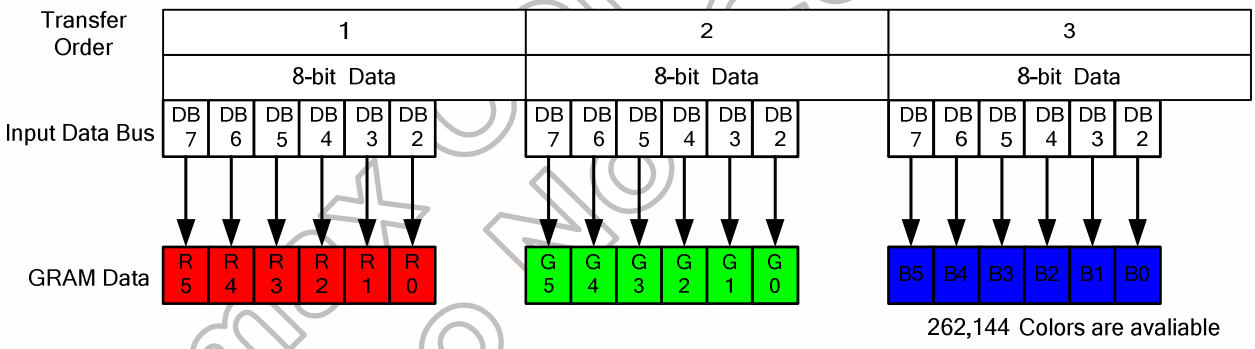

Figure 5. 13 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18(6 + 6 + 6) Bit-Data Input (“BS2, BS1, BS0”=”011”)

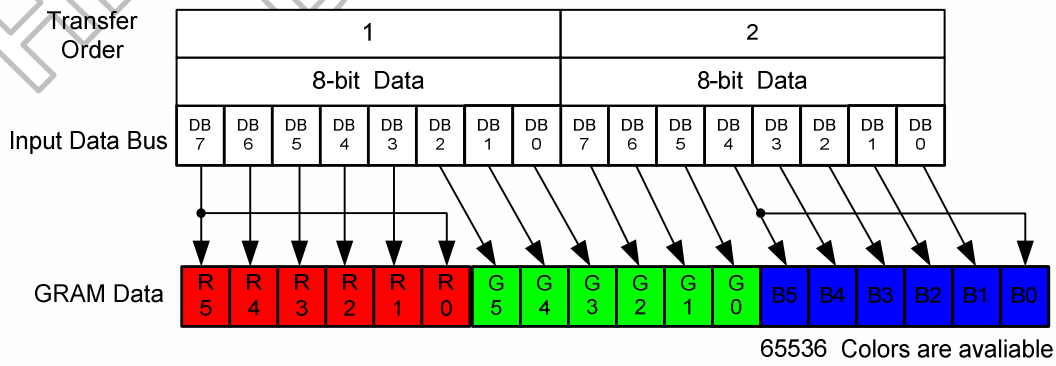

Figure 5. 14 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 16(5 + 6 + 5) Bit-Data Input (“BS2, BS1, BS0”=”100”)

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5.1.3 Serial bus system interface

The HX8352-A supports the serial bus interface in register-content mode by setting external pins “BS2, BS1” pins to “11”. The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), serial output data (SDO) and the serial transfer clock signal (DNC_SCL).

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code, register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin BS0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	RW	Function
0	0	Writes Indexes into IR
1	0	Writes command into register or data into GRAM
1	1	Reads command from register or data from GRAM

Table 5. 6 The Function of RS and R/W Bit bus

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A)TransferTiming Format in Serial Bus Interface for Index Register or Register Wirte

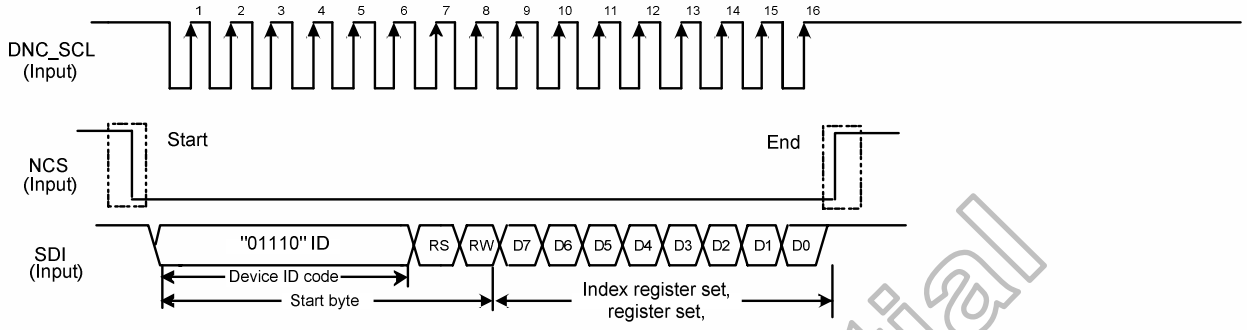

Figure 5. 15 Data Write Timing in Serial Bus System Interface

A)TransferTiming Format in Serial Bus Interface for Internal Status or Register Read

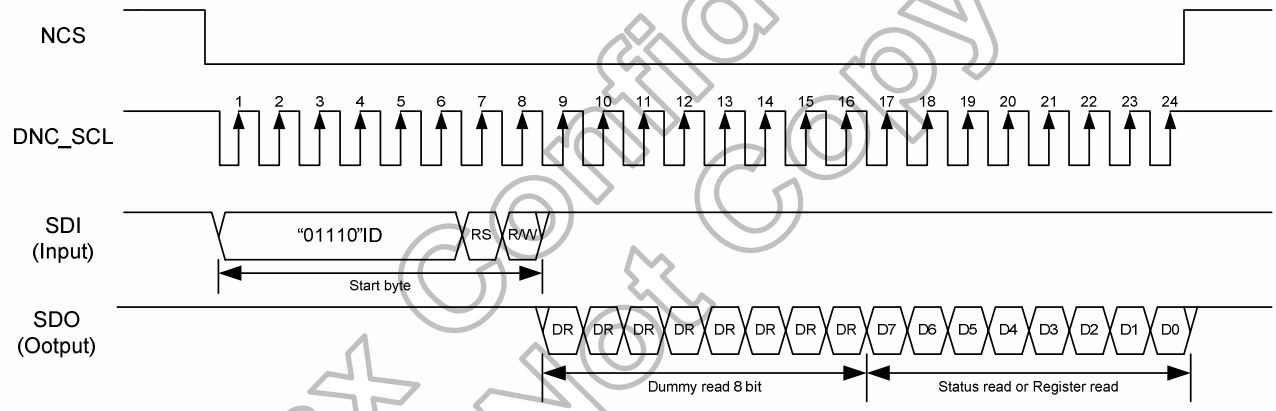

Figure 5. 16 Data Write Timing in Serial Bus System Interface

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5.1.4 RGB interface

The HX8352-A supports the RGB interface for writing animated display data. The RGB interface can be selected by setting external BS2-1 = 11. In RGB interface, the display operations is executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK), and the display data is inputted via RGB interface circuit without being written to the GRAM and display directly. The display data are transferred in pixel unit via D17-0 input pins. The display data input is latched on the rising edge of DOTCLK (DPL bit = 0) or the falling edge of DOTCLK (DPL bit = 1) by the chip when ENABLE signal is valid. Please refer to Table 5.7.

EPL	ENABLE	Display Data to Panel
0	1	Enable
0	0	Disable
1	1	Disable
1	0	Enable

Table 5. 7 EPL Bit Setting and Valid Enable Signal

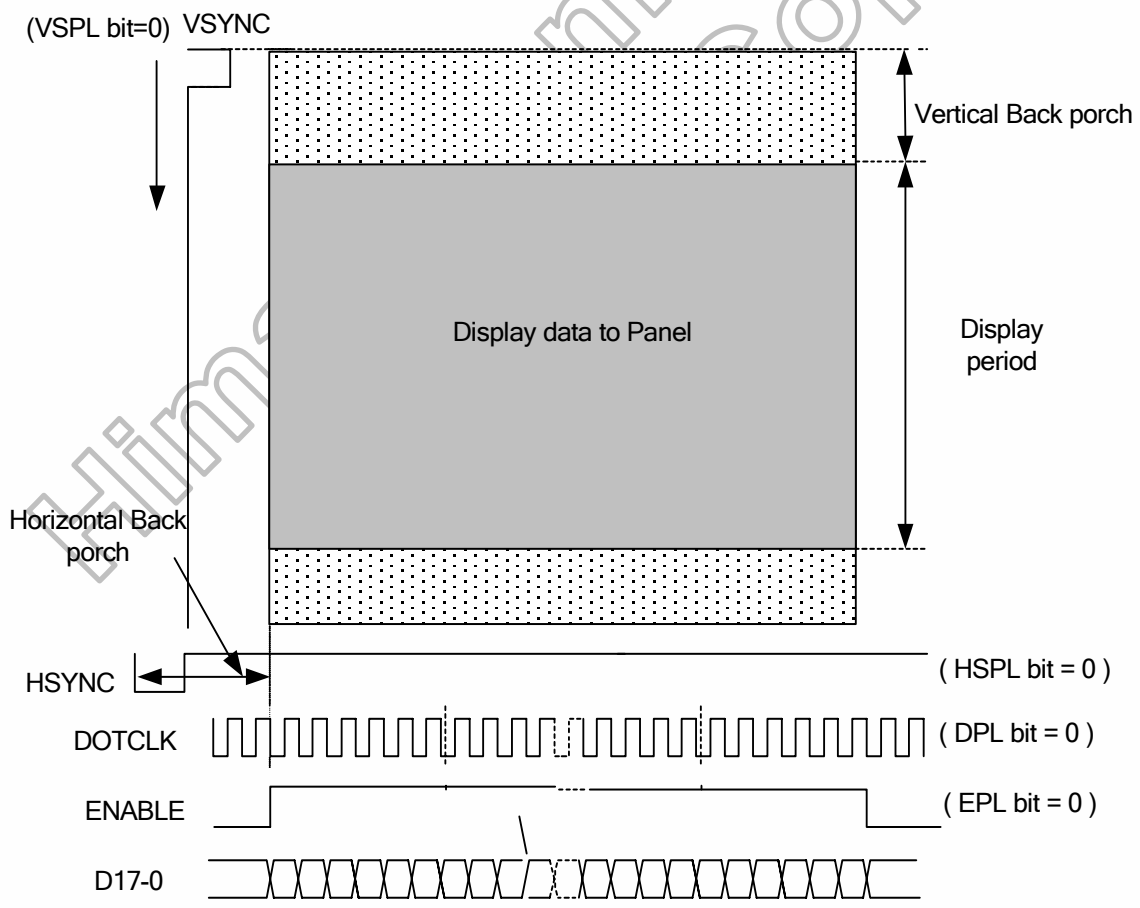

Figure 5. 17 RGB Interface Circuit Input Timing

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There are two types bit format per pixel color order for writing GRAM data in 18-bit bus interface selected by internal bits CSEL(2-0). The setting is shown in Figure5. 18 and Figure 5. 19.

(1) 16 bit/pixel color order (R 5-bit, G 6-bit, B 5-bit), 65,536 colors (CSEL(2-0) = "101")

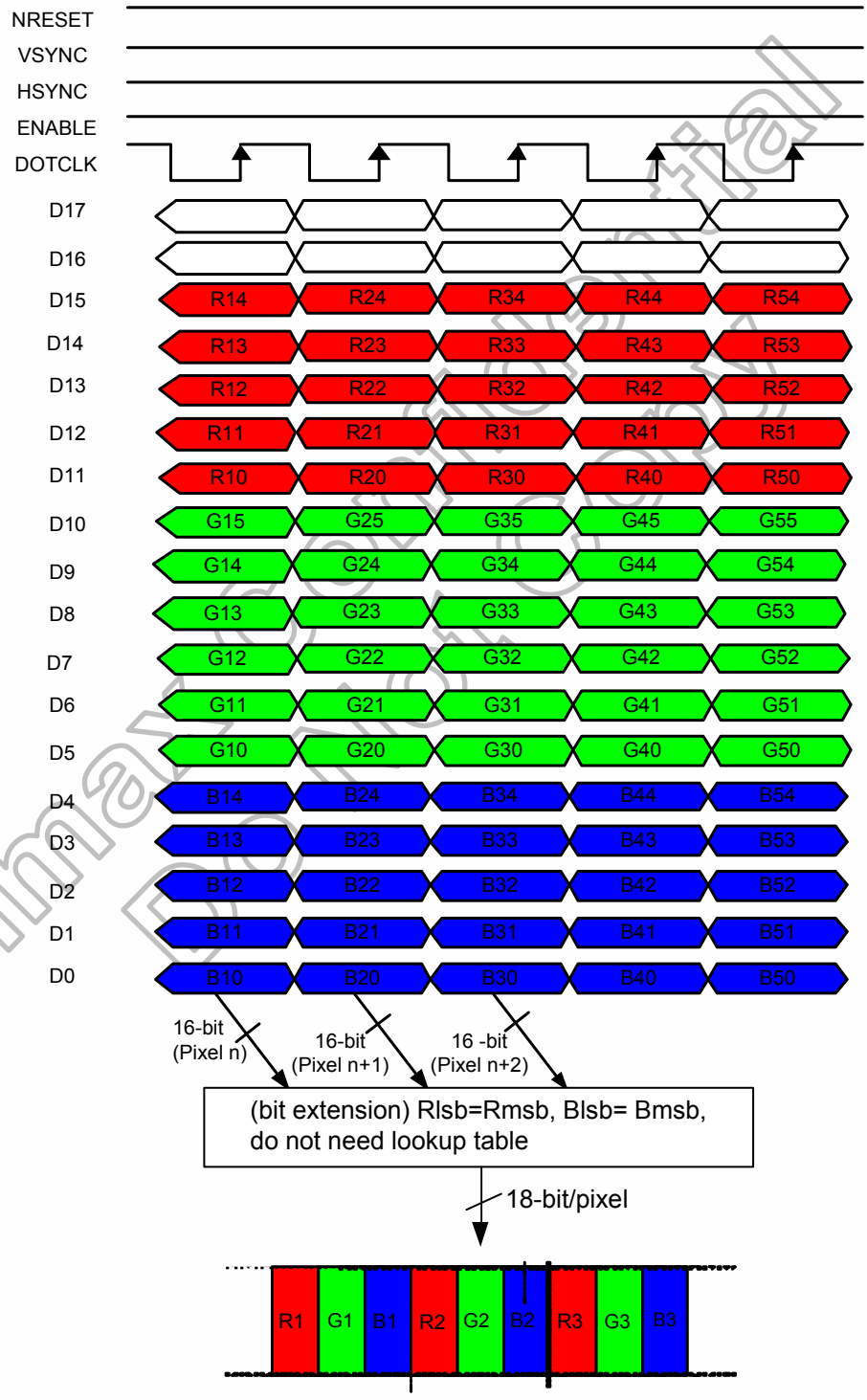

Figure 5. 18 16-Bit / Pixel Data Input of RGB Interface

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(2) 18 bit/pixel color order (R 6-bit, G 6-bit, B 6-bit), 262,144 colors (CSEL(2-0) = "110")

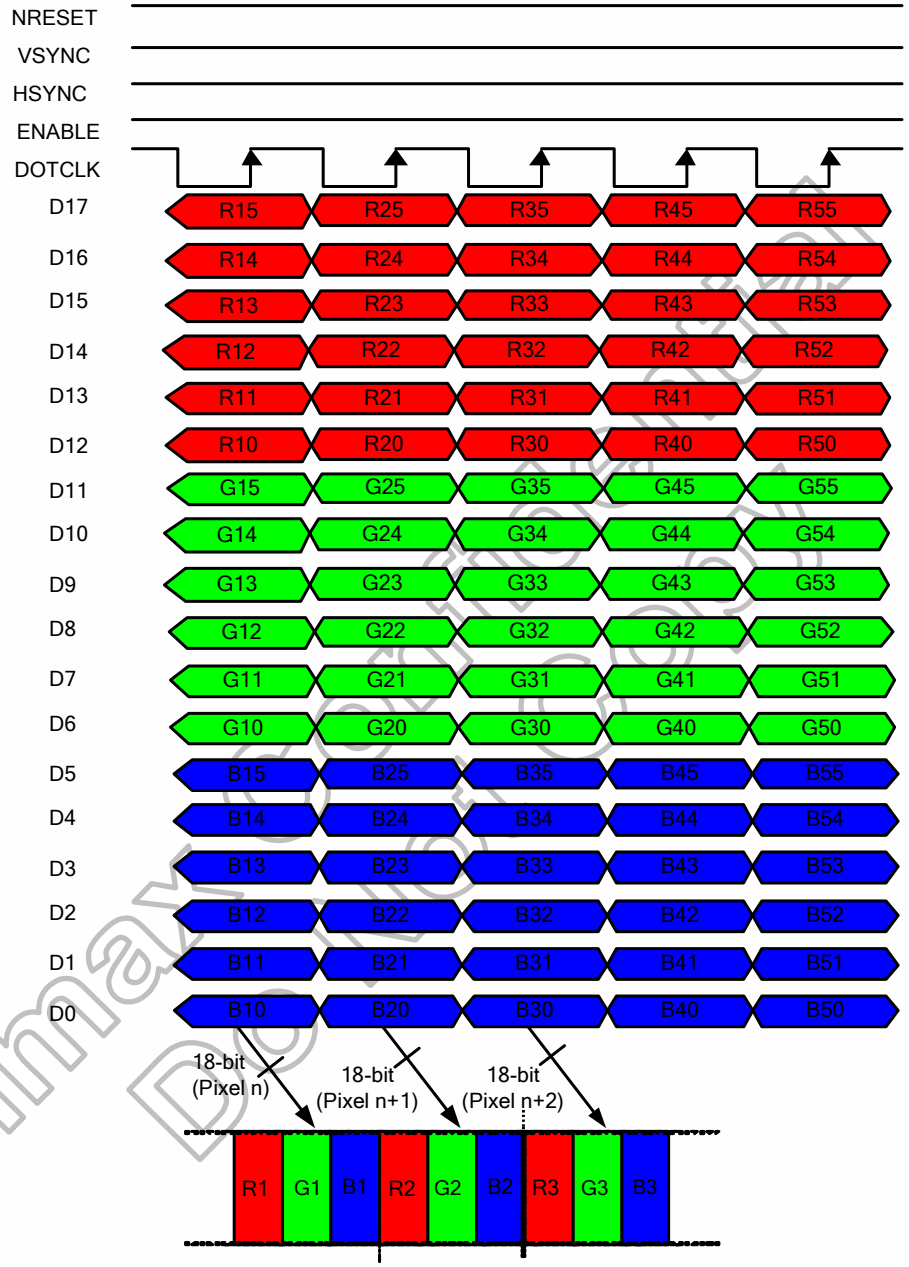

Figure 5. 19 18-Bit / Pixel Data Input of RGB Interface

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5.2 Address counter (AC)

The HX8352-A contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

RES_SEL1	RES_SEL0	X Range	Y Range	Panel Resolution
0	0	0~239d	0~319d.	240RGB x320 dot
0	1	0~239d	0~399d.	240RGB x400 dot
1	0	0~239d	0~431d.	240RGB x432 dot
1	1	0~239d	0~479d.	240RGB x480 dot

Table 5. 8 Addresses Counter Range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

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5.2.1 MCU to memory write/read direction

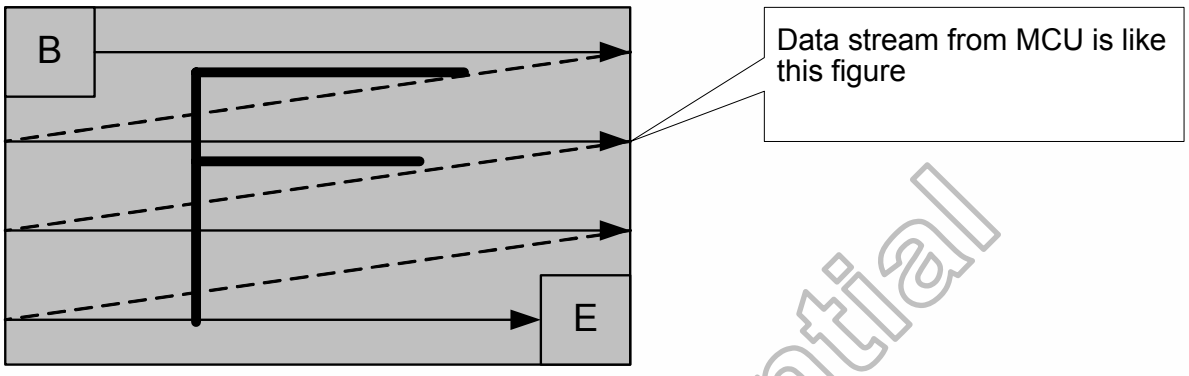

Figure 5. 20 MCU to Memory Write/Read Direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by “Memory Access Control” Command, Bits MY, MX, MV as described below.

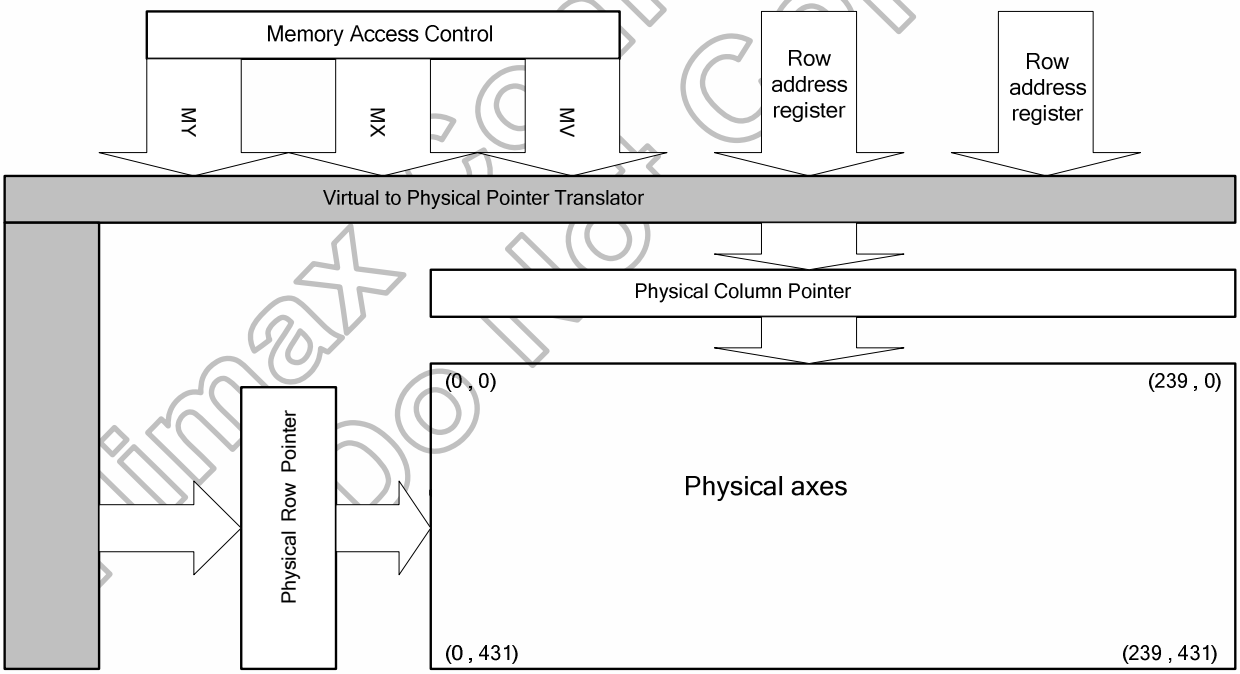

Figure 5. 21 MY, MX, MV Setting of 240RGB x 432 Dot

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (431-Physical Row Pointer) with SC
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (431-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (431-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (431-Physical Row Pointer)	Direct to (239-Physical Column Pointer)

Table 5. 9 MY, MX, MV Setting of 240RGB x 432 Dot

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The following figure depicts the update method set by MV, MX and MY bit.

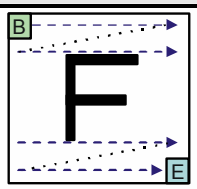
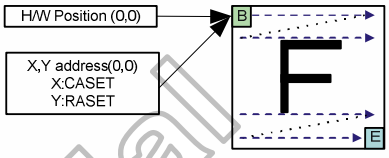
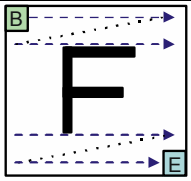
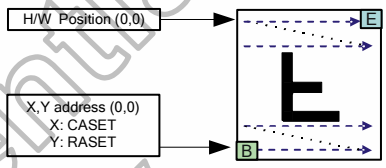
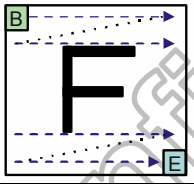
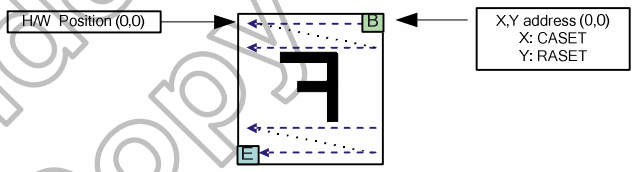
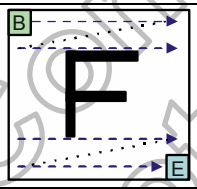
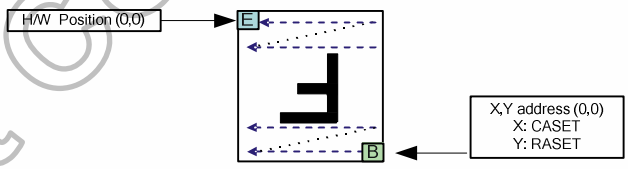
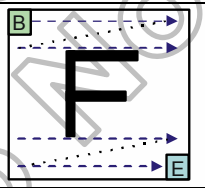
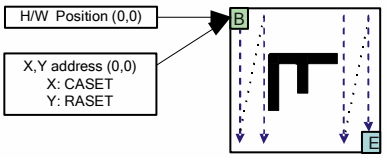
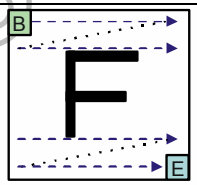
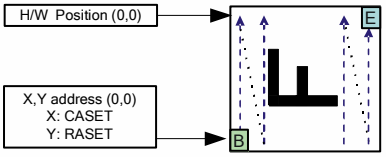
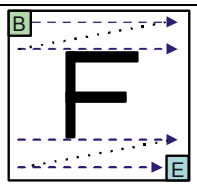
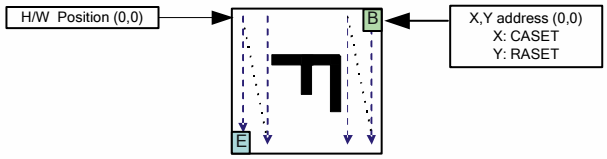
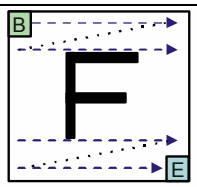
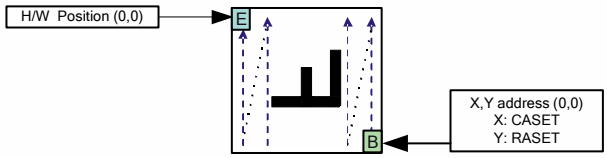
Display Data Direction	Memory Access Control			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

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Figure 5. 22 Address Direction Settings

5.3 Source, gate and memory map

Source Out		S1	S2	S3	S4	S5	S6	----------	S715	S716	S717	S718	S719	S720	Gate	
RA								RGB Order								
MY=0	MY=1							—— :BGR=0 ----- :BGR=1							GS=0	GS=1
0	431	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	–	R238 5-0	G238 5-0	B238 5-0	R239 5-0	G239 5-0	B239 5-0	G1	G432
1	430							–							G2	G431
2	429							–							G3	G430
3	428							–							G4	G429
4	427							–							G5	G428
5	426							–							G6	G427
6	425							–							G7	G426
7	424							–							G8	G425
8	423							–							G9	G424
9	422							–							G10	G423
10	421							–							G11	G422
11	420							–							G12	G421
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
424	7							–							G425	G8
425	6							–							G426	G7
426	5							–							G427	G6
427	4							–							G428	G5
428	3							–							G429	G4
429	2							–							G430	G3
430	1							–							G431	G2
431	0							–				RN 7-0	GN 7-0	BN 7-0	G432	G1
CA	MX=0	0			1				238			239				
	MX=1	239			238				1			0				

Display Pattern Data
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Note: **RA** = Row Address,
CA = Column Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control (R16h) command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control (R16h) command
GS = Scan direction parameter, D4 parameter of Memory Access Control (R16h) command
BGR = Red, Green and Blue pixel position change, D3 parameter of Memory Access Control (R16h) command

Figure 5. 23 Memory Map (240RGBx432)

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5.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.4.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

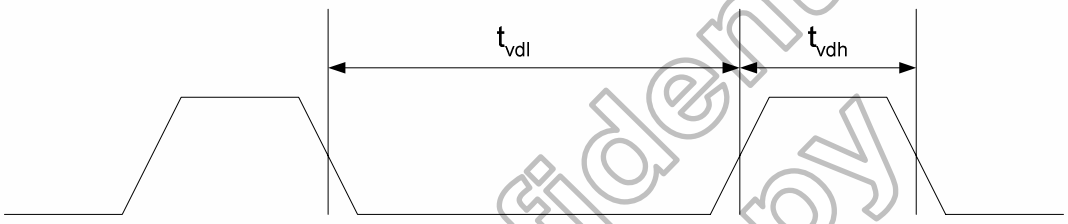


Figure 5. 24 TE Mode 1 Output

t_{vdh} = The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 (RES_SEL[1:0]=11) H-sync pulses per field.

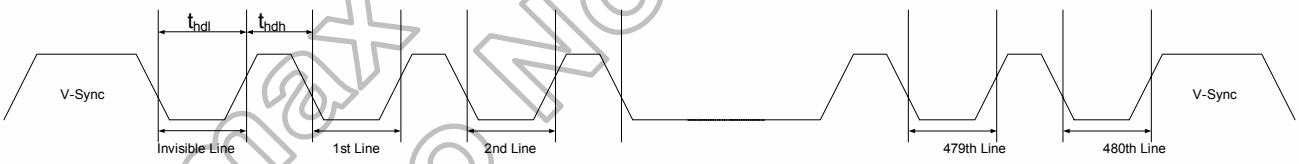
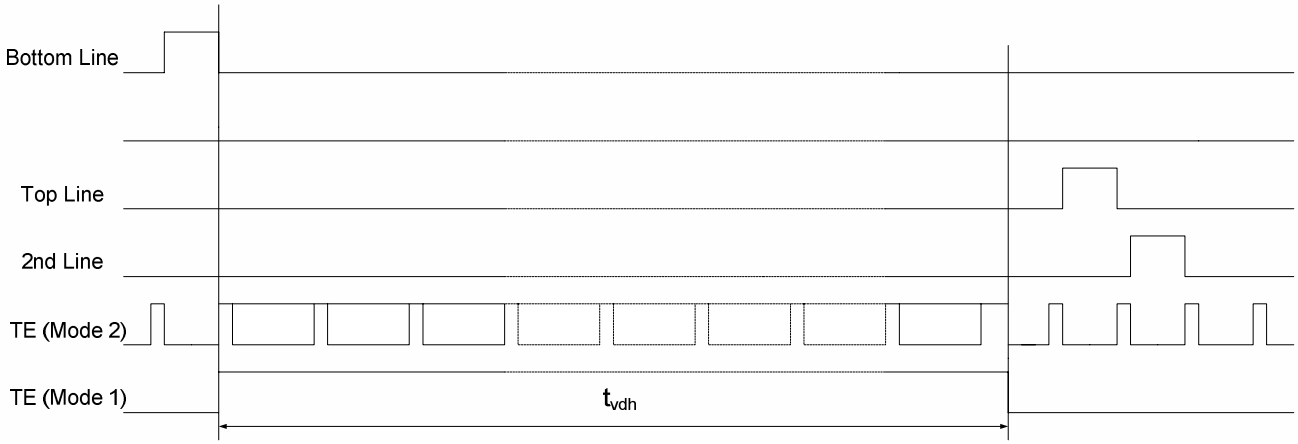


Figure 5. 25 TE Mode 2 Output

t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep in Mode, the Tearing Output Pin is active Low.

Figure 5. 26 TE Output Waveform

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5.4.2 Tearing effect line timing

The Tearing Effect signal is described below.

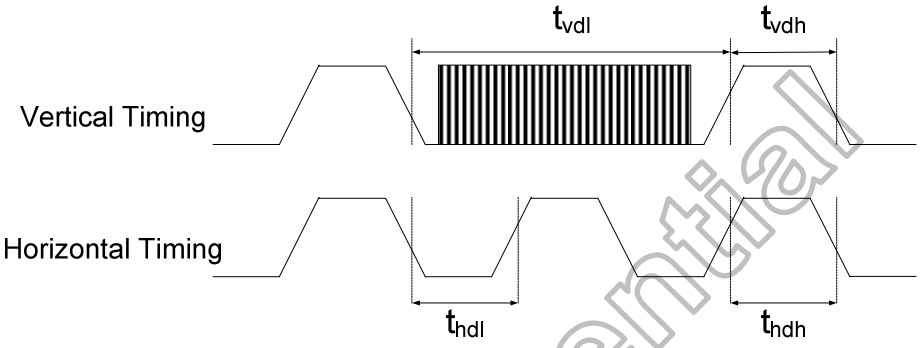

Figure 5. 27 Tearing Effect Signal Output

Idle Mode Off (Frame Rate = TBD Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	BP+FP	-	Line	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: (1) The timings in Table 5.13 apply when Memory Access Control GS=0 and GS=1.
(2) BP = Back porch, FP = Font porch.

Table 5. 10 AC Characteristics of Tearing Effect Signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

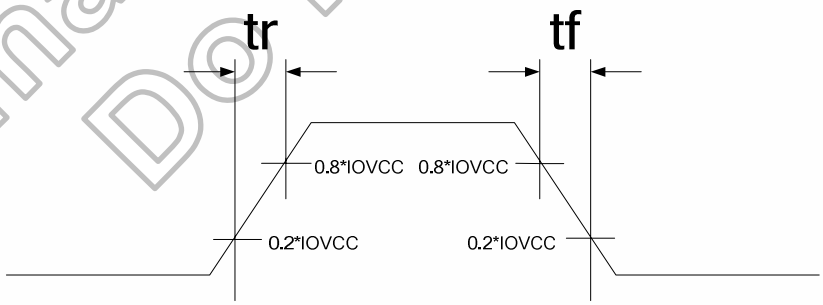

Figure 5. 28 AC Characteristics of Tearing Effect Signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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Example 1: MPU write is faster than panel read

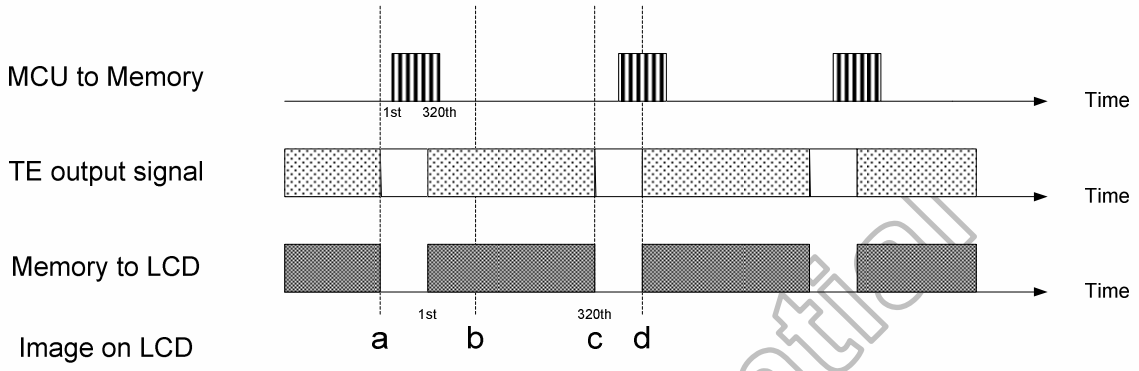

Figure 5. 29

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

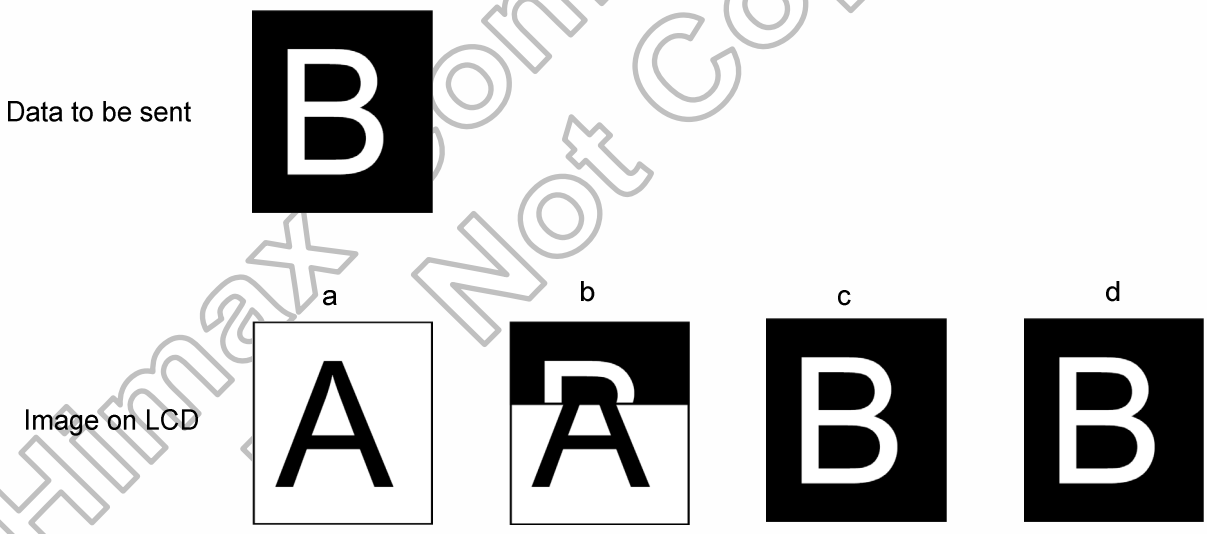

Figure 5. 30

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Example 2: MPU write is slower than panel read

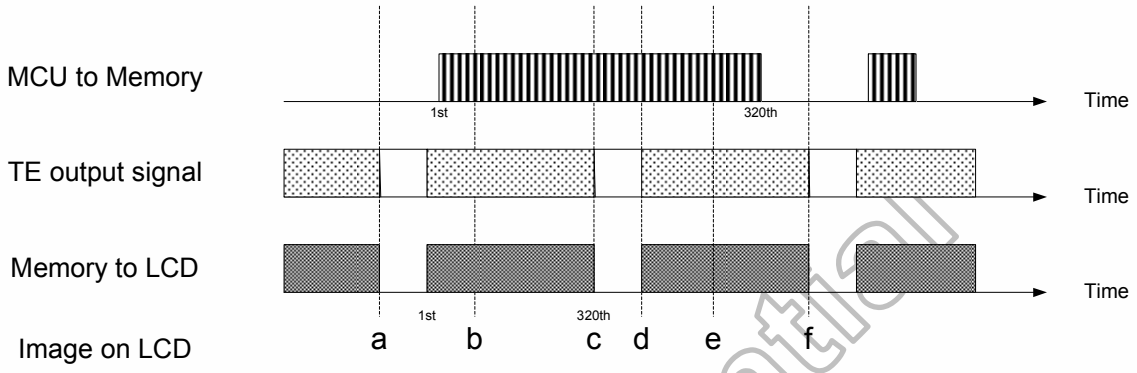

Figure 5. 31

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

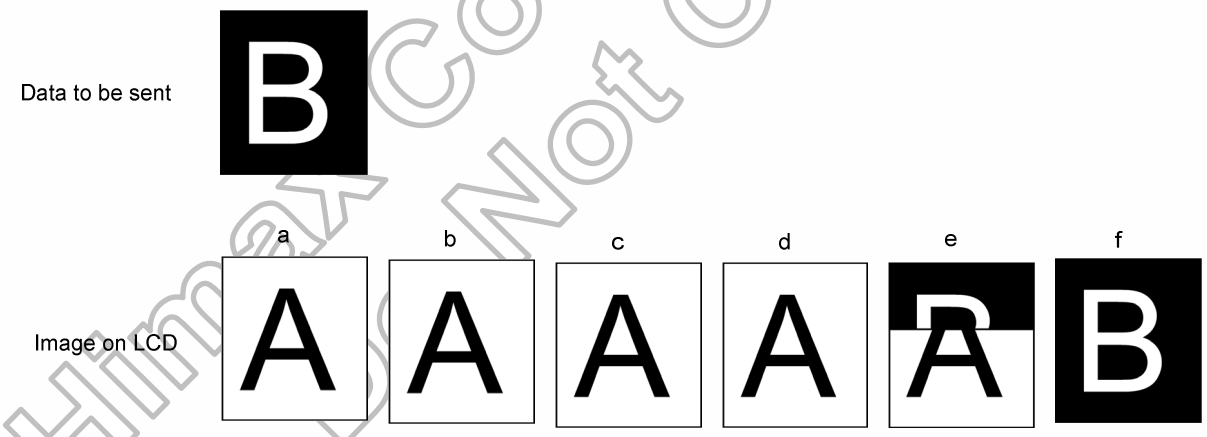

Figure 5. 32

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5.5 Oscillator

The HX8352-A can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the RADJ[3:0] internal register. Please refer to OSC control register (R17h). The default frequency is 7.5MHz.

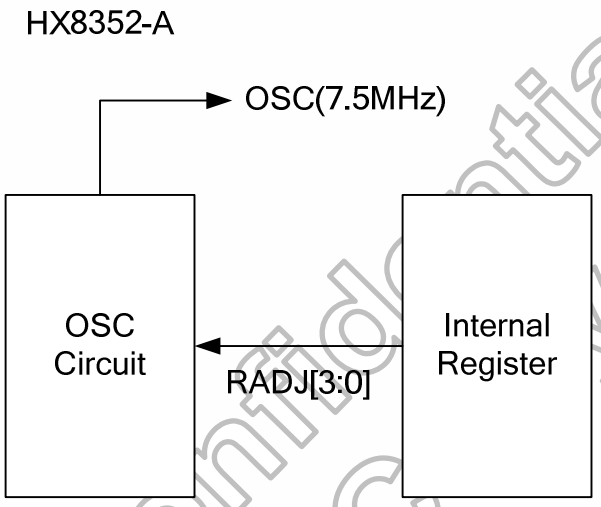

Figure 5. 33 Oscillation Circuit

5.6 Source driver

The HX8352-A contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.7 Gate driver

The HX8352-A contains a 480 gate channels of gate driver (G1~G480) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

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5.8 LCD power generation circuit

5.8.1 LCD power generation scheme

The boost voltage generated is shown as below.

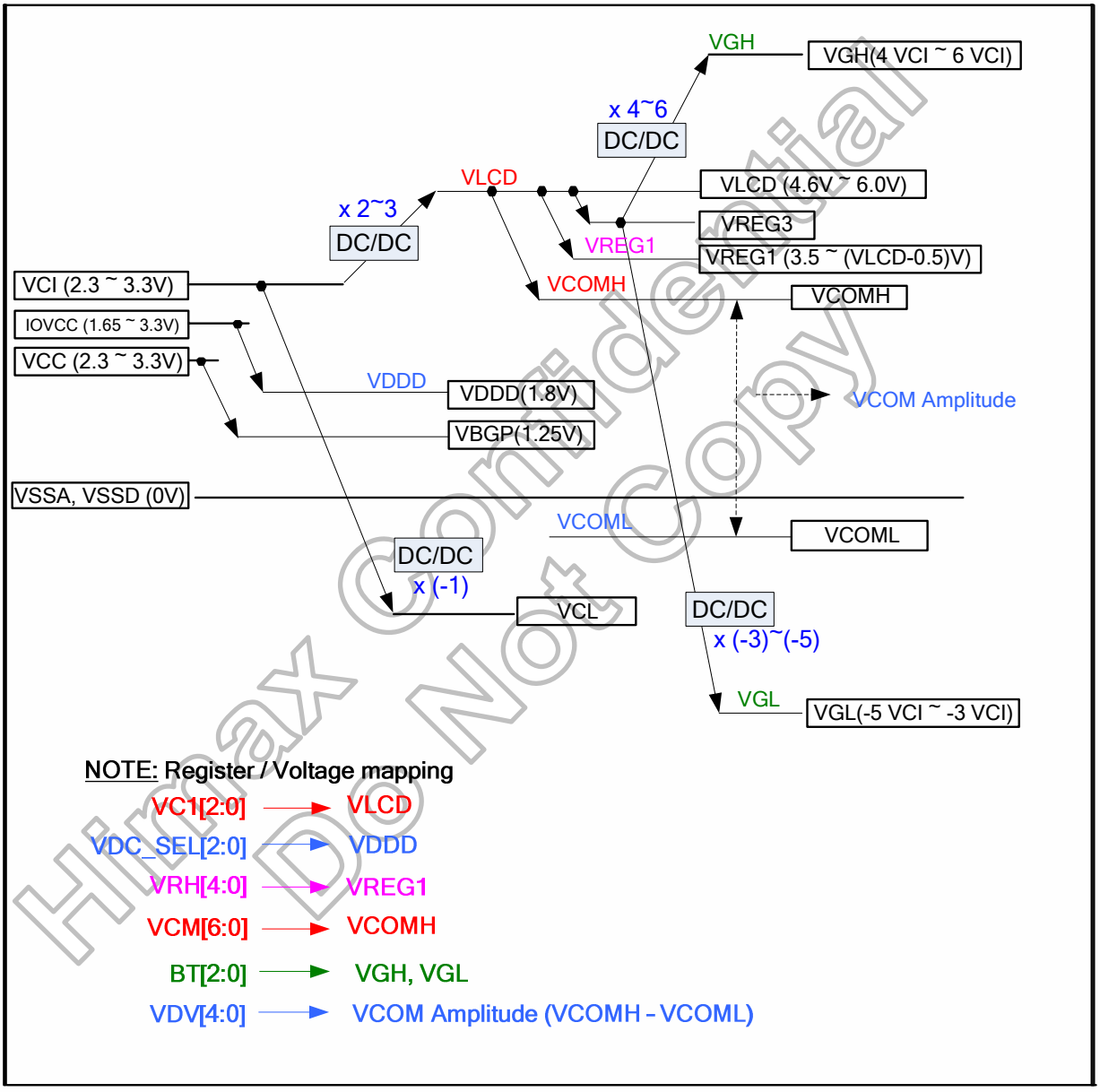

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Figure 5. 34 LCD Power Generation Scheme

5.8.2 Various boosting steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

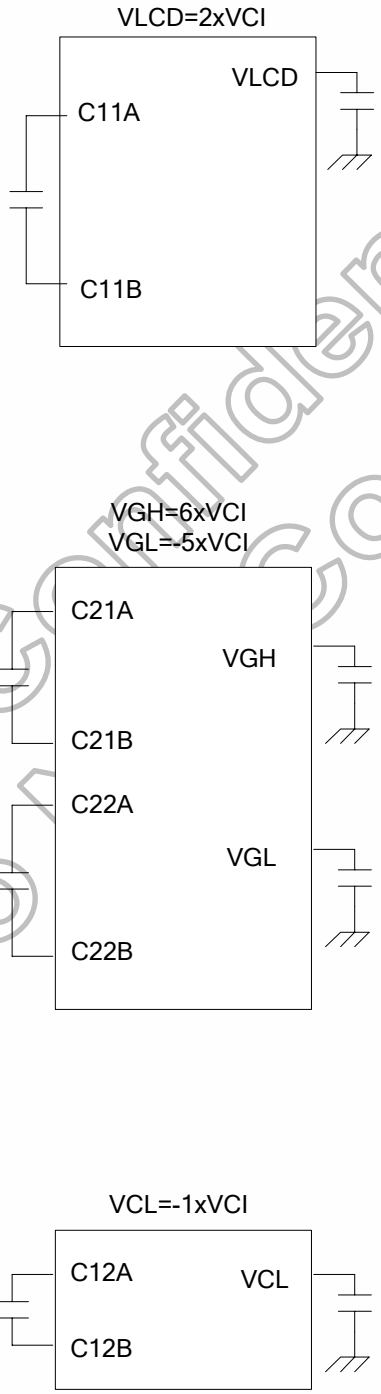

Figure 5. 35 Various Boosting Steps

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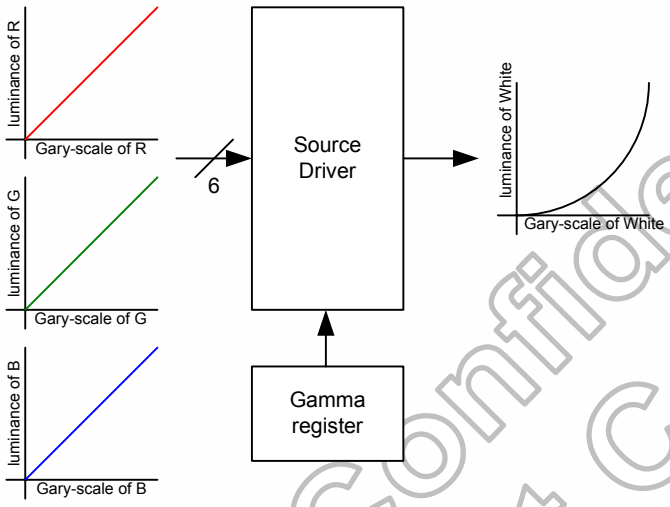
5.9 Gamma adjustment

The HX8352-A offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

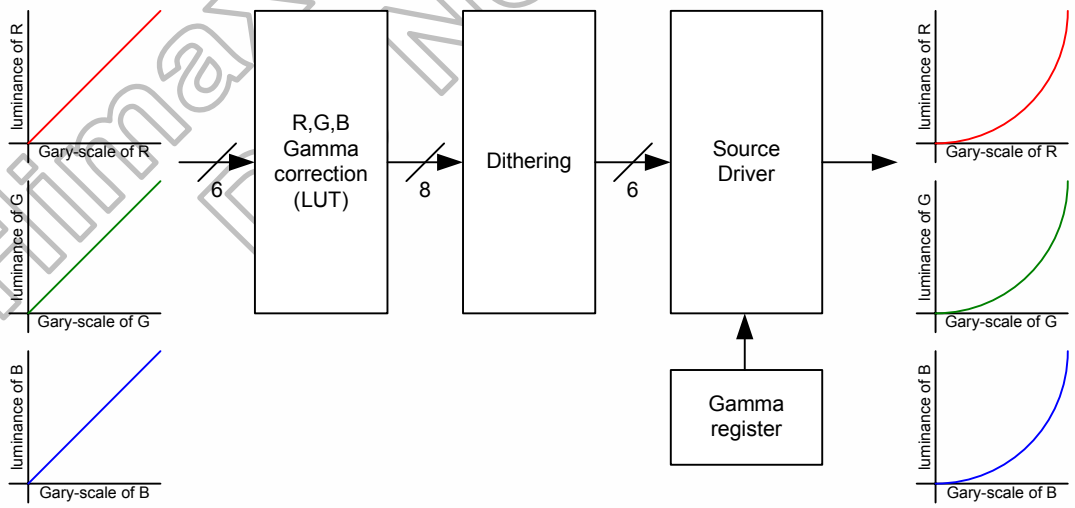


Figure 5. 36 Gamma Adjustments Different of Source Driver with Digital Gamma Correction

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5.9.1 Gray voltage generator for source driver

The HX8352-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

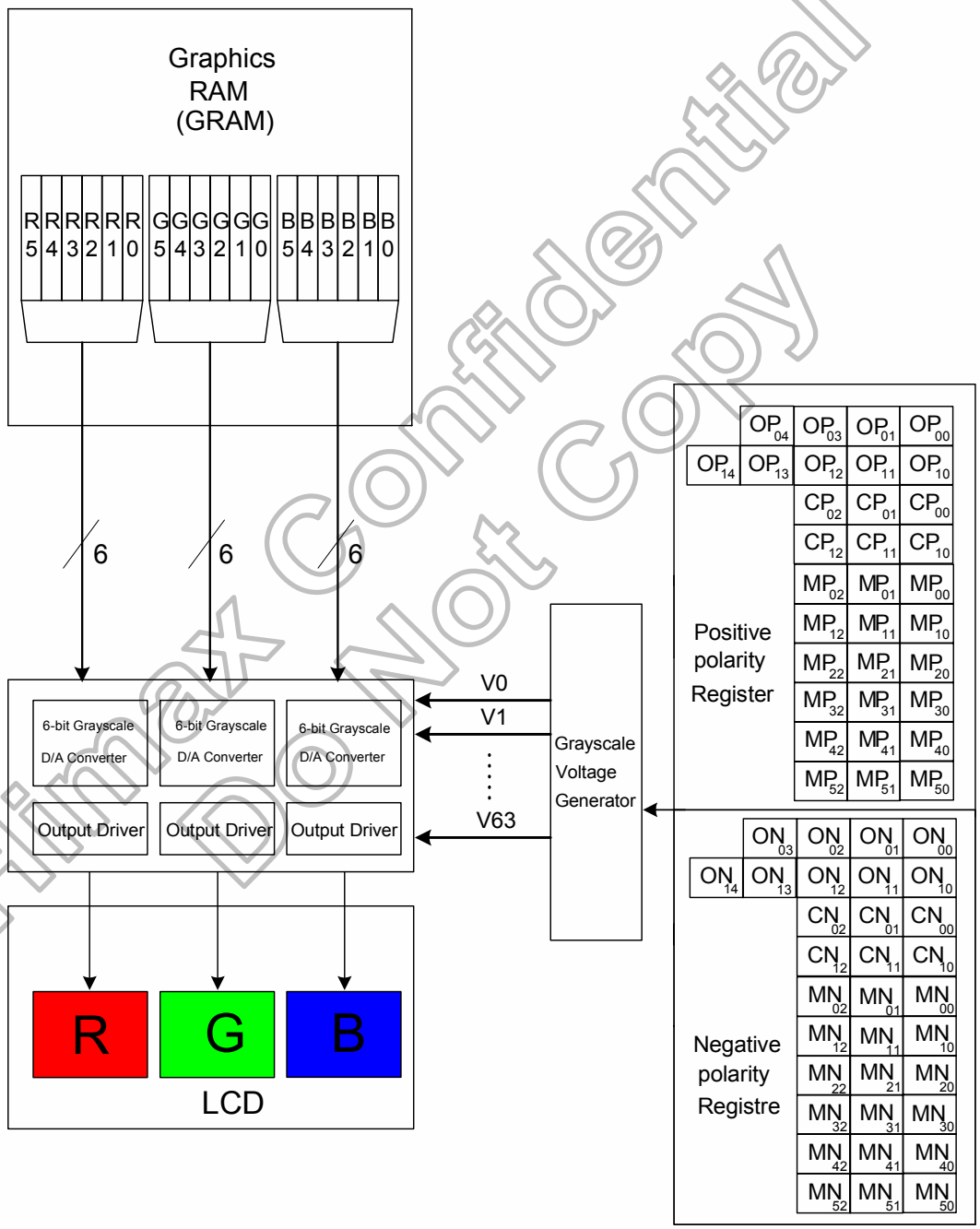

Figure 5. 37 Grayscale Control

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5.9.1.1 Structure of grayscale voltage generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, totally 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel.

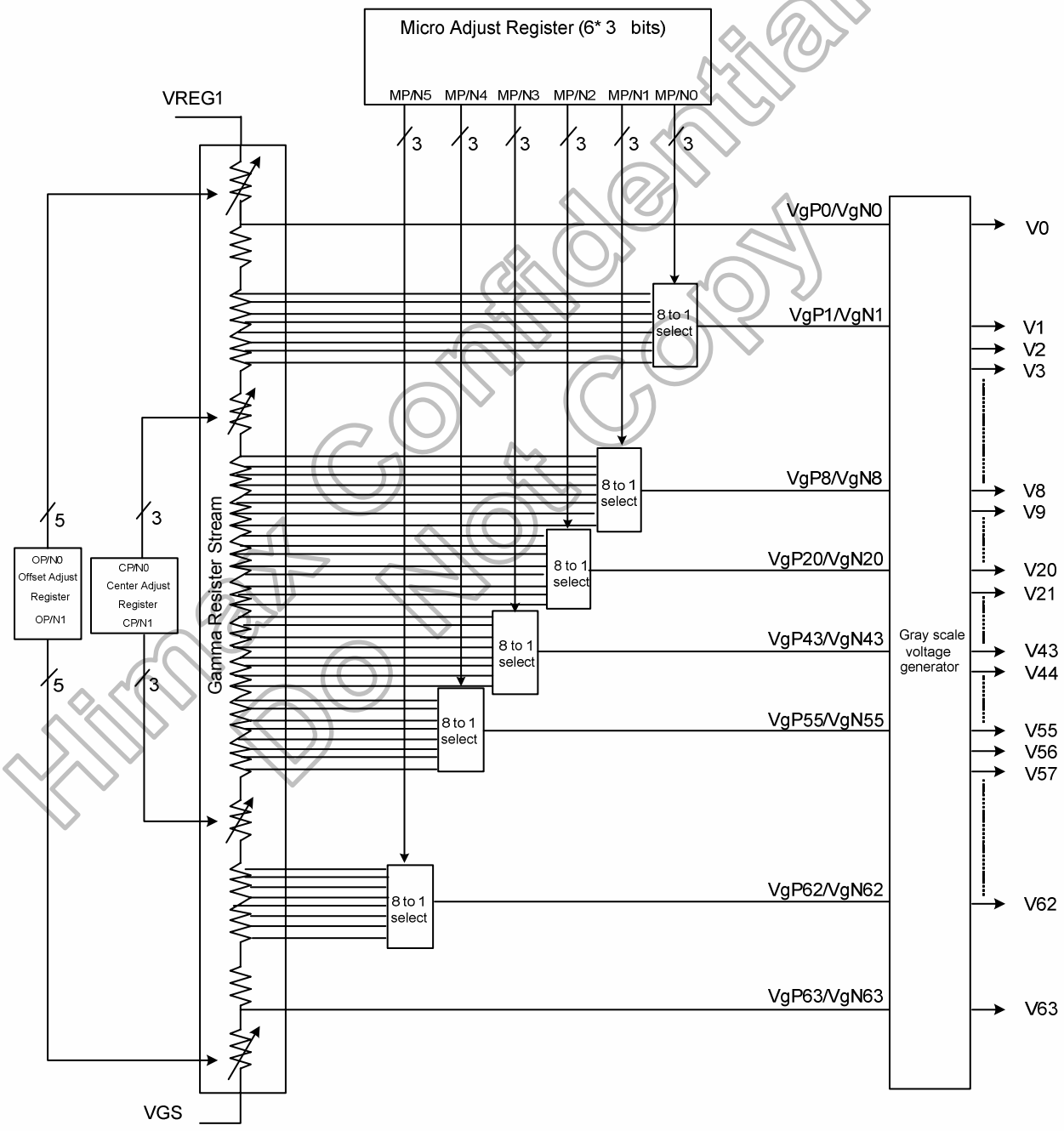

Figure 5. 38 Structure of Grayscale Voltage Generator

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5.9.1.2 Gamma-characteristics adjustment register

This HX8352-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

5.9.1.2.1 Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

5.9.1.2.2 Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

5.9.1.3 Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generates one reference voltage output (Vg(P/N)1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

Table 5. 11 Gamma-Adjustment Registers

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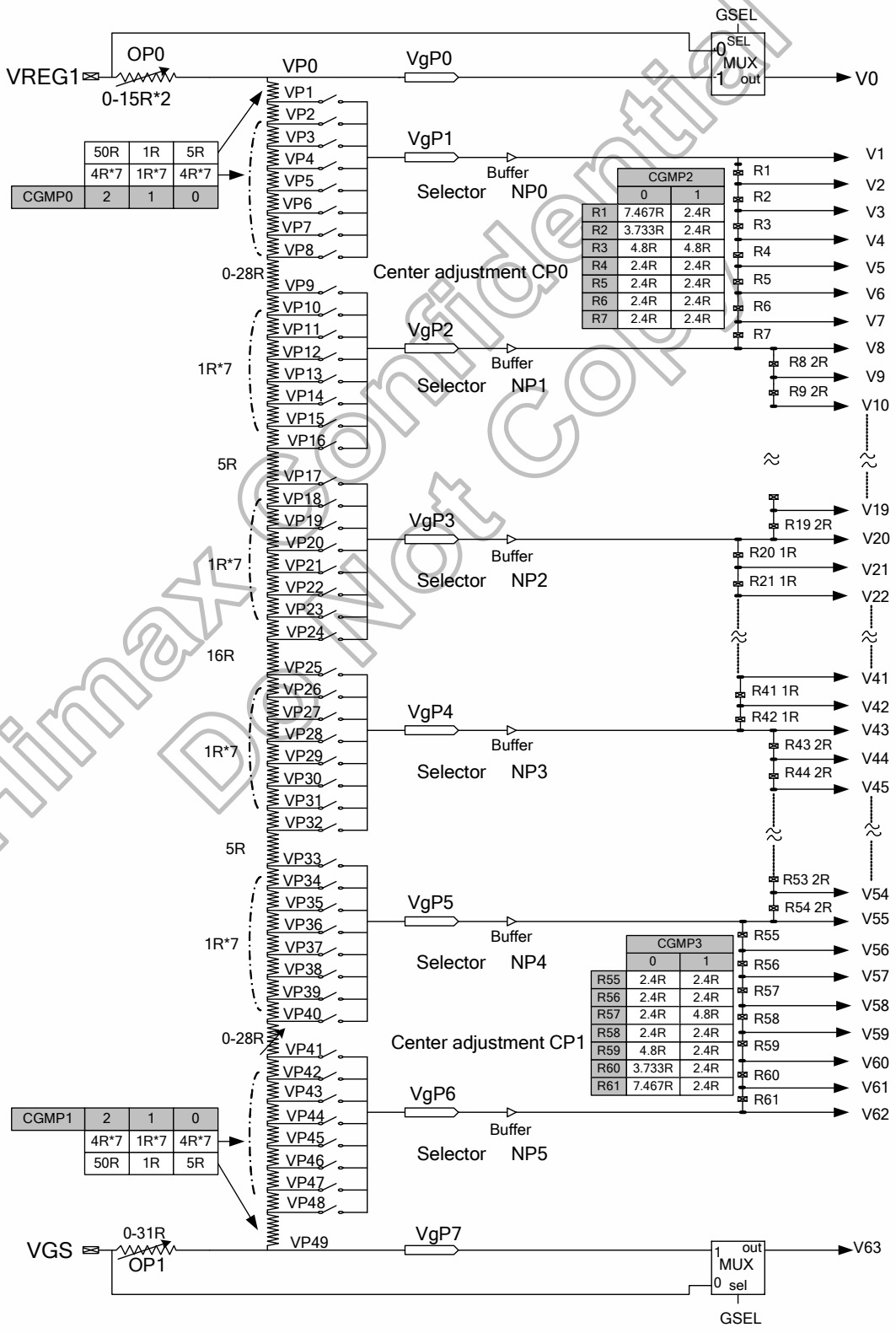
5.9.1.4 Gamma resister stream and 8 to 1 selector

The block consists of two gamma resister streams, one is for positive polarity and the other is for negative polarity, each one includes eight gamma reference voltages (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.



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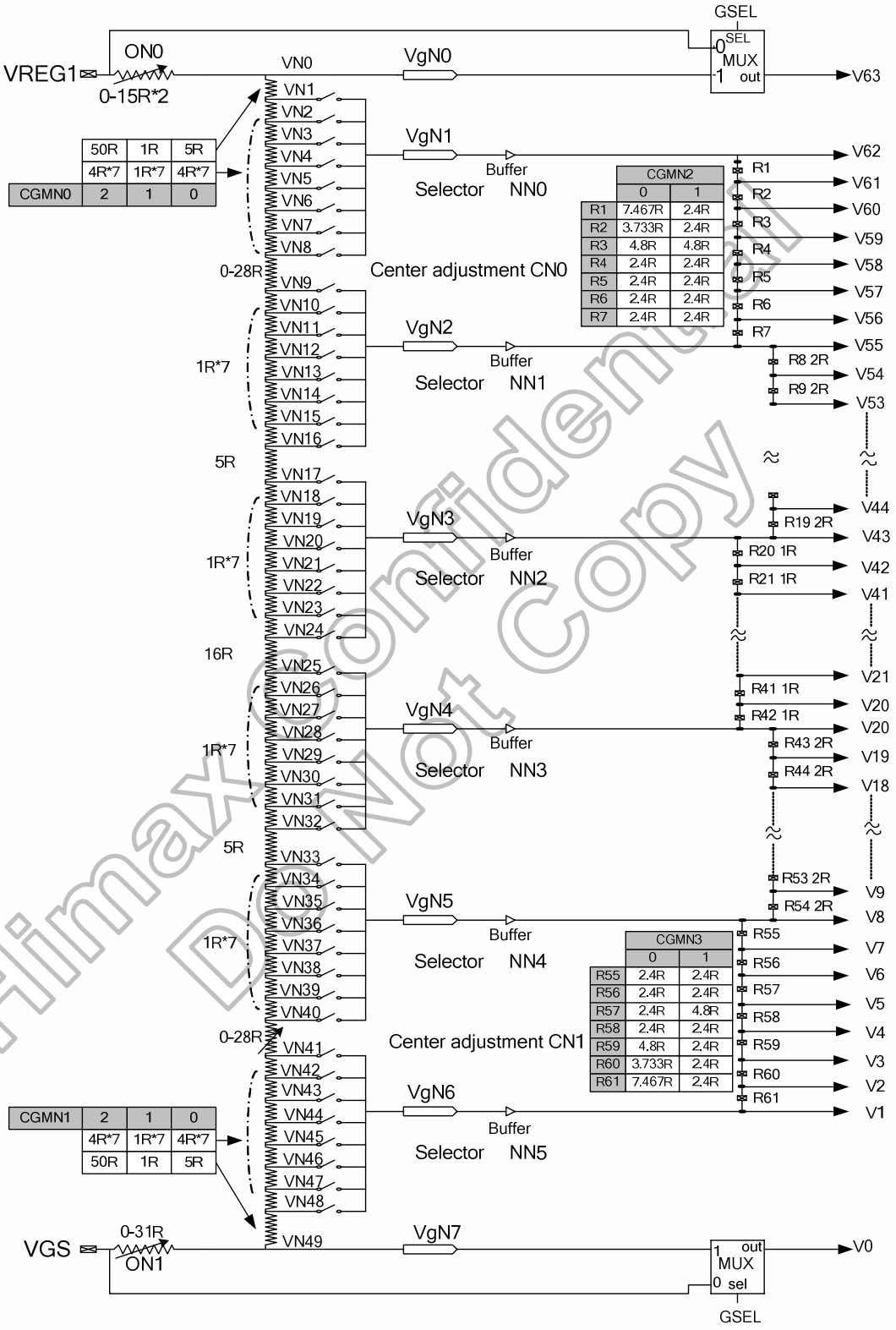

Figure 5. 39 Gamma Resister Stream and Gamma Reference Voltage

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5.9.1.5 Variable resister

There are two types of variable resistors, one is for center adjustment, the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown as below.

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5. 12 Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5. 13 Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)0/1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5. 14 Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream, and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown as below.

Value in Register	Voltage Level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 2	Vg(P/N) 3	Vg(P/N) 4	Vg(P/N) 5	Vg(P/N) 6
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5. 15 Output Voltage of 8 to 1 Selector

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The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	----	[(VREG1-VD*VROP0 /SumRP)] *GSEL +VREG1-(VREG1*GSEL)	VP0
VgP1	NP0 2-0=000	VREG1-VD[(VROP0+(CGMP0*1R)+5R- (CGMP0*5R)] /SumRP	VP1
	NP0 2-0=001	VREG1-VD[(VROP0+(CGMP0*2R)+9R- (CGMP0*9R)] /SumRP	VP2
	NP0 2-0=010	VREG1-VD[(VROP0+(CGMP0*3R)+13R- (CGMP0*13R)] /SumRP	VP3
	NP0 2-0=011	VREG1-VD[(VROP0+(CGMP0*4R)+17R- (CGMP0*17R)] /SumRP	VP4
	NP0 2-0=100	VREG1-VD[(VROP0+(CGMP0*5R)+21R- (CGMP0*21R)] /SumRP	VP5
	NP0 2-0=101	VREG1-VD[(VROP0+(CGMP0*6R)+25R- (CGMP0*25R)] /SumRP	VP6
	NP0 2-0=110	VREG1-VD[(VROP0+(CGMP0*7R)+29R- (CGMP0*29R)] /SumRP	VP7
	NP0 2-0=111	VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R)] /SumRP	VP8
VgP2	NP1 2-0=000	VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R) +VRCP0] /SumRP	VP9
	NP1 2-0=001	VREG1-VD[(VROP0+(CGMP0*9R)+34R- (CGMP0*34R) +VRCP0] /SumRP	VP10
	NP1 2-0=010	VREG1-VD[(VROP0+(CGMP0*10R)+35R- (CGMP0*35R) +VRCP0] /SumRP	VP11
	NP1 2-0=011	VREG1-VD[(VROP0+(CGMP0*11R)+36R- (CGMP0*36R) +VRCP0] /SumRP	VP12
	NP1 2-0=100	VREG1-VD[(VROP0+(CGMP0*12R)+37R- (CGMP0*37R) +VRCP0] /SumRP	VP13
	NP1 2-0=101	VREG1-VD[(VROP0+(CGMP0*13R)+38R- (CGMP0*38R) +VRCP0] /SumRP	VP14
	NP1 2-0=110	VREG1-VD[(VROP0+(CGMP0*14R)+39R- (CGMP0*39R) +VRCP0] /SumRP	VP15
	NP1 2-0=111	VREG1-VD[(VROP0+(CGMP0*15R)+40R- (CGMP0*40R) +VRCP0] /SumRP	VP16
VgP3	NP2 2-0=000	VREG1-VD[(VROP0+(CGMP0*20R)+45R- (CGMP0*45R) +VRCP0] /SumRP	VP17
	NP2 2-0=001	VREG1-VD[(VROP0+(CGMP0*21R)+46R- (CGMP0*46R) +VRCP0] /SumRP	VP18
	NP2 2-0=010	VREG1-VD[(VROP0+(CGMP0*22R)+47R- (CGMP0*47R) +VRCP0] /SumRP	VP19
	NP2 2-0=011	VREG1-VD[(VROP0+(CGMP0*23R)+48R- (CGMP0*48R) +VRCP0] /SumRP	VP20
	NP2 2-0=100	VREG1-VD[(VROP0+(CGMP0*24R)+49R- (CGMP0*49R) +VRCP0] /SumRP	VP21
	NP2 2-0=101	VREG1-VD[(VROP0+(CGMP0*25R)+50R- (CGMP0*50R) +VRCP0] /SumRP	VP22
	NP2 2-0=110	VREG1-VD[(VROP0+(CGMP0*26R)+51R- (CGMP0*51R) +VRCP0] /SumRP	VP23
	NP2 2-0=111	VREG1-VD[(VROP0+(CGMP0*27R)+52R- (CGMP0*52R) +VRCP0] /SumRP	VP24
VgP4	NP3 2-0=000	VREG1-VD[(VROP0+(CGMP0*43R)+68R- (CGMP0*68R) +VRCP0] /SumRP	VP25
	NP3 2-0=001	VREG1-VD[(VROP0+(CGMP0*44R)+69R- (CGMP0*69R) +VRCP0] /SumRP	VP26
	NP3 2-0=010	VREG1-VD[(VROP0+(CGMP0*45R)+70R- (CGMP0*70R) +VRCP0] /SumRP	VP27
	NP3 2-0=011	VREG1-VD[(VROP0+(CGMP0*46R)+71R- (CGMP0*71R) +VRCP0] /SumRP	VP28
	NP3 2-0=100	VREG1-VD[(VROP0+(CGMP0*47R)+72R- (CGMP0*72R) +VRCP0] /SumRP	VP29
	NP3 2-0=101	VREG1-VD[(VROP0+(CGMP0*48R)+73R- (CGMP0*73R) +VRCP0] /SumRP	VP30
	NP3 2-0=110	VREG1-VD[(VROP0+(CGMP0*49R)+74R- (CGMP0*74R) +VRCP0] /SumRP	VP31
	NP3 2-0=111	VREG1-VD[(VROP0+(CGMP0*50R)+75R- (CGMP0*75R) +VRCP0] /SumRP	VP32
VgP5	NP4 2-0=000	VREG1-VD[(VROP0+(CGMP0*55R)+80R- (CGMP0*80R) +VRCP0] /SumRP	VP33
	NP4 2-0=001	VREG1-VD[(VROP0+(CGMP0*56R)+81R- (CGMP0*81R) +VRCP0] /SumRP	VP34
	NP4 2-0=010	VREG1-VD[(VROP0+(CGMP0*57R)+82R- (CGMP0*82R) +VRCP0] /SumRP	VP35
	NP4 2-0=011	VREG1-VD[(VROP0+(CGMP0*58R)+83R- (CGMP0*83R) +VRCP0] /SumRP	VP36
	NP4 2-0=100	VREG1-VD[(VROP0+(CGMP0*59R)+84R- (CGMP0*84R) +VRCP0] /SumRP	VP37
	NP4 2-0=101	VREG1-VD[(VROP0+(CGMP0*60R)+85R- (CGMP0*85R) +VRCP0] /SumRP	VP38
	NP4 2-0=110	VREG1-VD[(VROP0+(CGMP0*61R)+86R- (CGMP0*86R) +VRCP0] /SumRP	VP39
	NP4 2-0=111	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0] /SumRP	VP40
VgP6	NP5 2-0=000	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1] /SumRP	VP41
	NP5 2-0=001	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+4R-(4R*CGMP1)+(CGMP1*1R)] /SumRP	VP42
	NP5 2-0=010	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+8R-(8R*CGMP1)+(CGMP1*2R)] /SumRP	VP43
	NP5 2-0=011	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+12R-(12R*CGMP1)+(CGMP1*3R)] /SumRP	VP44
	NP5 2-0=100	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+16R-(16R*CGMP1)+(CGMP1*4R)] /SumRP	VP45
	NP5 2-0=101	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+20R-(20R*CGMP1)+(CGMP1*5R)] /SumRP	VP46
	NP5 2-0=110	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+24R-(24R*CGMP1)+(CGMP1*6R)] /SumRP	VP47
	NP5 2-0=111	VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+28R-(28R*CGMP1)+(CGMP1*7R)] /SumRP	VP48
VgP7	----	{ VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R) +VRCP0+VRCP1+33R-(33R*CGMP1)+(CGMP1*8R)] /SumRP } *GSEL+VGS-(GSEL*VGS)	VP49

Note: CGMP0=1 or 0, CGMP1=1 or 0.
SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1*25R)-(CGMP0*25R);
SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1*25R)-(CGMN0*25R)
VD=(VREG1-VGS)

Table 5. 16 Voltage Calculation Formula (Positive Polarity)

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Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgP0	V32	VgP4+(VgP3-VgP4)*(11/23)
V1	VgP1	V33	VgP4+(VgP3-VgP4)*(10/23)
V2	VgP2+(VgP1-VgP2)*(CGMP2*14.4/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(18.133/25.6)	V34	VgP4+(VgP3-VgP4)*(9/23)
V3	VgP2+(VgP1-VgP2)*(CGMP2*12/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(4.4/25.6)	V35	VgP4+(VgP3-VgP4)*(8/23)
V4	VgP2+(VgP1-VgP2)*(CGMP2*9.6/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(9.6/25.6)	V36	VgP4+(VgP3-VgP4)*(7/23)
V5	VgP2+(VgP1-VgP2)*(CGMP2*7.2/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(7.2/25.6)	V37	VgP4+(VgP3-VgP4)*(6/23)
V6	VgP2+(VgP1-VgP2)*(CGMP2*4.8/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(4.8/25.6)	V38	VgP4+(VgP3-VgP4)*(5/23)
V7	VgP2+(VgP1-VgP2)*(CGMP2*2.4/16.8)+ (VgP1-VgP2)*(1-CGMP2)*(2.4/25.6)	V39	VgP4+(VgP3-VgP4)*(4/23)
V8	VgP2	V40	VgP4+(VgP3-VgP4)*(3/23)
V9	VgP3+(VgP2-VgP3)*(22/24)	V41	VgP4+(VgP3-VgP4)*(2/23)
V10	VgP3+(VgP2-VgP3)*(20/24)	V42	VgP4+(VgP3-VgP4)*(1/23)
V11	VgP3+(VgP2-VgP3)*(18/24)	V43	VgP4
V12	VgP3+(VgP2-VgP3)*(16/24)	V44	VgP5+(VgP4-VgP5)*(22/24)
V13	VgP3+(VgP2-VgP3)*(14/24)	V45	VgP5+(VgP4-VgP5)*(20/24)
V14	VgP3+(VgP2-VgP3)*(12/24)	V46	VgP5+(VgP4-VgP5)*(18/24)
V15	VgP3+(VgP2-VgP3)*(10/24)	V47	VgP5+(VgP4-VgP5)*(16/24)
V16	VgP3+(VgP2-VgP3)*(8/24)	V48	VgP5+(VgP4-VgP5)*(14/24)
V17	VgP3+(VgP2-VgP3)*(6/24)	V49	VgP5+(VgP4-VgP5)*(12/24)
V18	VgP3+(VgP2-VgP3)*(4/24)	V50	VgP5+(VgP4-VgP5)*(10/24)
V19	VgP3+(VgP2-VgP3)*(2/24)	V51	VgP5+(VgP4-VgP5)*(8/24)
V20	VgP3	V52	VgP5+(VgP4-VgP5)*(6/24)
V21	VgP4+(VgP3-VgP4)*(22/23)	V53	VgP5+(VgP4-VgP5)*(4/24)
V22	VgP4+(VgP3-VgP4)*(21/23)	V54	VgP5+(VgP4-VgP5)*(2/24)
V23	VgP4+(VgP3-VgP4)*(20/23)	V55	VgP5
V24	VgP4+(VgP3-VgP4)*(19/23)	V56	VgP6+(VgP5-VgP6)*(CGMP3*14.4/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(23.2/25.6)
V25	VgP4+(VgP3-VgP4)*(18/23)	V57	VgP6+(VgP5-VgP6)*(CGMP3*12/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(20.8/25.6)
V26	VgP4+(VgP3-VgP4)*(17/23)	V58	VgP6+(VgP5-VgP6)*(CGMP3*9.6/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(18.4/25.6)
V27	VgP4+(VgP3-VgP4)*(16/23)	V59	VgP6+(VgP5-VgP6)*(CGMP3*7.2/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(16/25.6)
V28	VgP4+(VgP3-VgP4)*(15/23)	V60	VgP6+(VgP5-VgP6)*(CGMP3*4.8/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(11.2/25.6)
V29	VgP4+(VgP3-VgP4)*(14/23)	V61	VgP6+(VgP5-VgP6)*(CGMP3*2.4/16.8)+ (VgP5-VgP6)*(1-CGMP3)*(7.467/25.6)
V30	VgP4+(VgP3-VgP4)*(13/23)	V62	VgP6
V31	VgP4+(VgP3-VgP4)*(12/23)	V63	VgP7

Table 5. 17 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

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Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	[(VREG1-VD*VRON0 /SumRN)] *GSEL +VREG1-(VREG1*GSEL)	VN0
VgN1	NN0 2-0=000	VREG1-VD[(VRON0+(CGMN0*1R)+5R- (CGMN0*5R)] /SumRN	VN1
	NN0 2-0=001	VREG1-VD[(VRON0+(CGMN0*2R)+9R- (CGMN0*9R)] /SumRN	VN2
	NN0 2-0=010	VREG1-VD[(VRON0+(CGMN0*3R)+13R- (CGMN0*13R)] /SumRN	VN3
	NN0 2-0=011	VREG1-VD[(VRON0+(CGMN0*4R)+17R- (CGMN0*17R)] /SumRN	VN4
	NN0 2-0=100	VREG1-VD[(VRON0+(CGMN0*5R)+21R- (CGMN0*21R)] /SumRN	VN5
	NN0 2-0=101	VREG1-VD[(VRON0+(CGMN0*6R)+25R- (CGMN0*25R)] /SumRN	VN6
	NN0 2-0=110	VREG1-VD[(VRON0+(CGMN0*7R)+29R- (CGMN0*29R)] /SumRN	VN7
	NN0 2-0=111	VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R)] /SumRN	VN8
VgN2	NN1 2-0=000	VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R) +VRCN0] /SumRN	VN9
	NN1 2-0=001	VREG1-VD[(VRON0+(CGMN0*9R)+34R- (CGMN0*34R) +VRCN0] /SumRN	VN10
	NN1 2-0=010	VREG1-VD[(VRON0+(CGMN0*10R)+35R- (CGMN0*35R) +VRCN0] /SumRN	VN11
	NN1 2-0=011	VREG1-VD[(VRON0+(CGMN0*11R)+36R- (CGMN0*36R) +VRCN0] /SumRN	VN12
	NN1 2-0=100	VREG1-VD[(VRON0+(CGMN0*12R)+37R- (CGMN0*37R) +VRCN0] /SumRN	VN13
	NN1 2-0=101	VREG1-VD[(VRON0+(CGMN0*13R)+38R- (CGMN0*38R) +VRCN0] /SumRN	VN14
	NN1 2-0=110	VREG1-VD[(VRON0+(CGMN0*14R)+39R- (CGMN0*39R) +VRCN0] /SumRN	VN15
	NN1 2-0=111	VREG1-VD[(VRON0+(CGMN0*15R)+40R- (CGMN0*40R) +VRCN0] /SumRN	VN16
VgN3	NN2 2-0=000	VREG1-VD[(VRON0+(CGMN0*20R)+45R- (CGMN0*45R) +VRCN0] /SumRN	VN17
	NN2 2-0=001	VREG1-VD[(VRON0+(CGMN0*21R)+46R- (CGMN0*46R) +VRCN0] /SumRN	VN18
	NN2 2-0=010	VREG1-VD[(VRON0+(CGMN0*22R)+47R- (CGMN0*47R) +VRCN0] /SumRN	VN19
	NN2 2-0=011	VREG1-VD[(VRON0+(CGMN0*23R)+48R- (CGMN0*48R) +VRCN0] /SumRN	VN20
	NN2 2-0=100	VREG1-VD[(VRON0+(CGMN0*24R)+49R- (CGMN0*49R) +VRCN0] /SumRN	VN21
	NN2 2-0=101	VREG1-VD[(VRON0+(CGMN0*25R)+50R- (CGMN0*50R) +VRCN0] /SumRN	VN22
	NN2 2-0=110	VREG1-VD[(VRON0+(CGMN0*26R)+51R- (CGMN0*51R) +VRCN0] /SumRN	VN23
	NN2 2-0=111	VREG1-VD[(VRON0+(CGMN0*27R)+52R- (CGMN0*52R) +VRCN0] /SumRN	VN24
VgN4	NN3 2-0=000	VREG1-VD[(VRON0+(CGMN0*43R)+68R- (CGMN0*68R) +VRCN0] /SumRN	VN25
	NN3 2-0=001	VREG1-VD[(VRON0+(CGMN0*44R)+69R- (CGMN0*69R) +VRCN0] /SumRN	VN26
	NN3 2-0=010	VREG1-VD[(VRON0+(CGMN0*45R)+70R- (CGMN0*70R) +VRCN0] /SumRN	VN27
	NN3 2-0=011	VREG1-VD[(VRON0+(CGMN0*46R)+71R- (CGMN0*71R) +VRCN0] /SumRN	VNP8
	NN3 2-0=100	VREG1-VD[(VRON0+(CGMN0*47R)+72R- (CGMN0*72R) +VRCN0] /SumRN	VN29
	NN3 2-0=101	VREG1-VD[(VRON0+(CGMN0*48R)+73R- (CGMN0*73R) +VRCN0] /SumRN	VN30
	NN3 2-0=110	VREG1-VD[(VRON0+(CGMN0*49R)+74R- (CGMN0*74R) +VRCN0] /SumRN	VN31
	NN3 2-0=111	VREG1-VD[(VRON0+(CGMN0*50R)+75R- (CGMN0*75R) +VRCN0] /SumRN	VN32
VgN5	NN4 2-0=000	VREG1-VD[(VRON0+(CGMN0*55R)+80R- (CGMN0*80R) +VRCN0] /SumRN	VN33
	NN4 2-0=001	VREG1-VD[(VRON0+(CGMN0*56R)+81R- (CGMN0*81R) +VRCN0] /SumRN	VN34
	NN4 2-0=010	VREG1-VD[(VRON0+(CGMN0*57R)+82R- (CGMN0*82R) +VRCN0] /SumRN	VN35
	NN4 2-0=011	VREG1-VD[(VRON0+(CGMN0*58R)+83R- (CGMN0*83R) +VRCN0] /SumRN	VN36
	NN4 2-0=100	VREG1-VD[(VRON0+(CGMN0*59R)+84R- (CGMN0*84R) +VRCN0] /SumRN	VN37
	NN4 2-0=101	VREG1-VD[(VRON0+(CGMN0*60R)+85R- (CGMN0*85R) +VRCN0] /SumRN	VN38
	NN4 2-0=110	VREG1-VD[(VRON0+(CGMN0*61R)+86R- (CGMN0*86R) +VRCN0] /SumRN	VN39
	NN4 2-0=111	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0] /SumRN	VN40
VgN6	NN5 2-0=000	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1] /SumRN	VN41
	NN5 2-0=001	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+4R-(4R*CGMN1)+(CGMN1*1R)] /SumRN	VN42
	NN5 2-0=010	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+8R-(8R*CGMN1)+(CGMN1*2R)] /SumRN	VN43
	NN5 2-0=011	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+12R-(12R*CGMN1)+(CGMN1*3R)] /SumRN	VN44
	NN5 2-0=100	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+16R-(16R*CGMN1)+(CGMN1*4R)] /SumRN	VN45
	NN5 2-0=101	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+20R-(20R*CGMN1)+(CGMN1*5R)] /SumRN	VN46
	NN5 2-0=110	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+24R-(24R*CGMN1)+(CGMN1*6R)] /SumRN	VN47
	NN5 2-0=111	VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+28R-(28R*CGMN1)+(CGMN1*7R)] /SumRN	VN48
VgN7	-	{ VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+33R-(33R*CGMN1)+(CGMN1*8R)]/SumRN } *GSEL+VGS-(GSEL*VGS)	VN49

Note: CGMN0=1 or 0, CGMN1=1 or 0
SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1*25R)-(CGMP0*25R);
SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1*25R)-(CGMN0*25R)
VD=(VREG1-VGS)

Table 5. 18 Voltage Calculation Formula (Negative Polarity)

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Grayscale Voltage	Formula
V63	VgN0
V62	VgN1
V61	VgN2+(VgN1-VgN2)*(CGMN2*14.4/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(18.133/25.6)
V60	VgN2+(VgN1-VgN2)*(CGMN2*12/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(14.4/25.6)
V59	VgN2+(VgN1-VgN2)*(CGMN2*9.6/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(9.6/25.6)
V58	VgN2+(VgN1-VgN2)*(CGMN2*7.2/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(7.2/25.6)
V57	VgN2+(VgN1-VgN2)*(CGMN2*4.8/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(4.8/25.6)
V56	VgN2+(VgN1-VgN2)*(CGMN2*2.4/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(2.4/25.6)
V55	VgN2
V54	VgN3+(VgN2-VgN3)*(22/24)
V53	VgN3+(VgN2-VgN3)*(20/24)
V52	VgN3+(VgN2-VgN3)*(18/24)
V51	VgN3+(VgN2-VgN3)*(16/24)
V50	VgN3+(VgN2-VgN3)*(14/24)
V49	VgN3+(VgN2-VgN3)*(12/24)
V48	VgN3+(VgN2-VgN3)*(10/24)
V47	VgN3+(VgN2-VgN3)*(8/24)
V46	VgN3+(VgN2-VgN3)*(6/24)
V45	VgN3+(VgN2-VgN3)*(4/24)
V44	VgN3+(VgN2-VgN3)*(2/24)
V43	VgN3
V42	VgN4+(VgN3-VgN4)*(22/23)
V41	VgN4+(VgN3-VgN4)*(21/23)
V40	VgN4+(VgN3-VgN4)*(20/23)
V39	VgN4+(VgN3-VgN4)*(19/23)
V38	VgN4+(VgN3-VgN4)*(18/23)
V37	VgN4+(VgN3-VgN4)*(17/23)
V36	VgN4+(VgN3-VgN4)*(16/23)
V35	VgN4+(VgN3-VgN4)*(15/23)
V34	VgN4+(VgN3-VgN4)*(14/23)
V33	VgN4+(VgN3-VgN4)*(13/23)
V32	VgN4+(VgN3-VgN4)*(12/23)

Grayscale Voltage	Formula
V31	VgN4+(VgN3-VgN4)*(11/23)
V30	VgN4+(VgN3-VgN4)*(10/23)
V29	VgN4+(VgN3-VgN4)*(9/23)
V28	VgN4+(VgN3-VgN4)*(8/23)
V27	VgN4+(VgN3-VgN4)*(7/23)
V26	VgN4+(VgN3-VgN4)*(6/23)
V25	VgN4+(VgN3-VgN4)*(5/23)
V24	VgN4+(VgN3-VgN4)*(4/23)
V23	VgN4+(VgN3-VgN4)*(3/23)
V22	VgN4+(VgN3-VgN4)*(2/23)
V21	VgN4+(VgN3-VgN4)*(1/23)
V20	VgN4
V19	VgN5+(VgN4-VgN5)*(22/24)
V18	VgN5+(VgN4-VgN5)*(20/24)
V17	VgN5+(VgN4-VgN5)*(18/24)
V16	VgN5+(VgN4-VgN5)*(16/24)
V15	VgN5+(VgN4-VgN5)*(14/24)
V14	VgN5+(VgN4-VgN5)*(12/24)
V13	VgN5+(VgN4-VgN5)*(10/24)
V12	VgN5+(VgN4-VgN5)*(8/24)
V11	VgN5+(VgN4-VgN5)*(6/24)
V10	VgN5+(VgN4-VgN5)*(4/24)
V9	VgN5+(VgN4-VgN5)*(2/24)
V8	VgN5
V7	VgN6+(VgN5-VgN6)*(CGMN3*14.4/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(23.2/25.6)
V6	VgN6+(VgN5-VgN6)*(CGMN3*12/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(20.8/25.6)
5	VgN6+(VgN5-VgN6)*(CGMN3*9.6/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(18.4/25.6)
V4	VgN6+(VgN5-VgN6)*(CGMN3*7.2/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(16/25.6)
V3	VgN6+(VgN5-VgN6)*(CGMN3*4.8/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(11.2/25.6)
V2	VgN6+(VgN5-VgN6)*(CGMN3*2.4/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(7.467/25.6)
V1	VgN6
V0	VgN7

Table 5. 19 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

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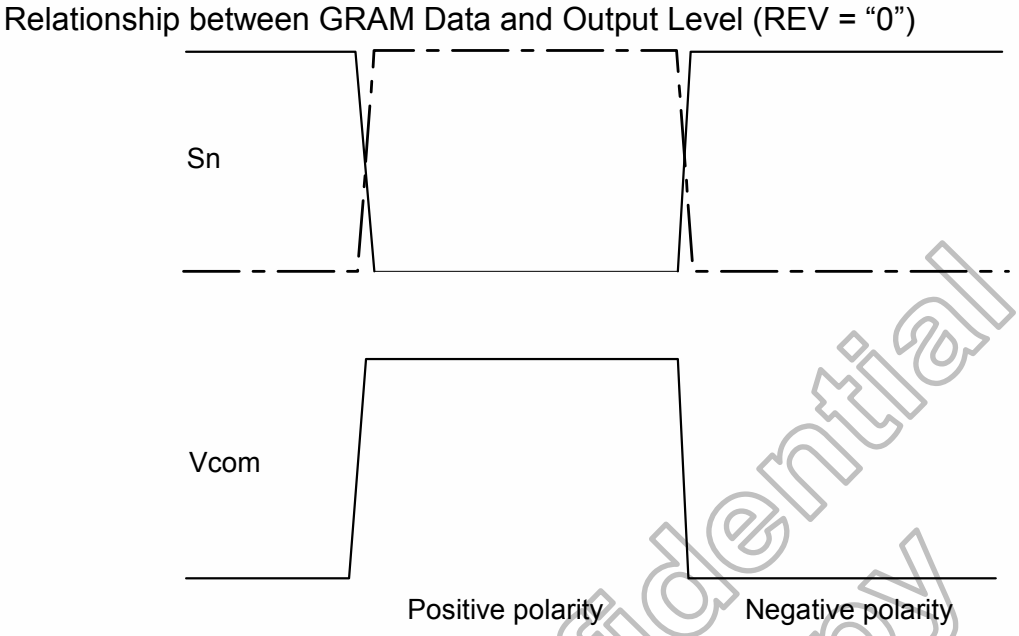

Figure 5. 40 Relationship between Source Output and Vcom

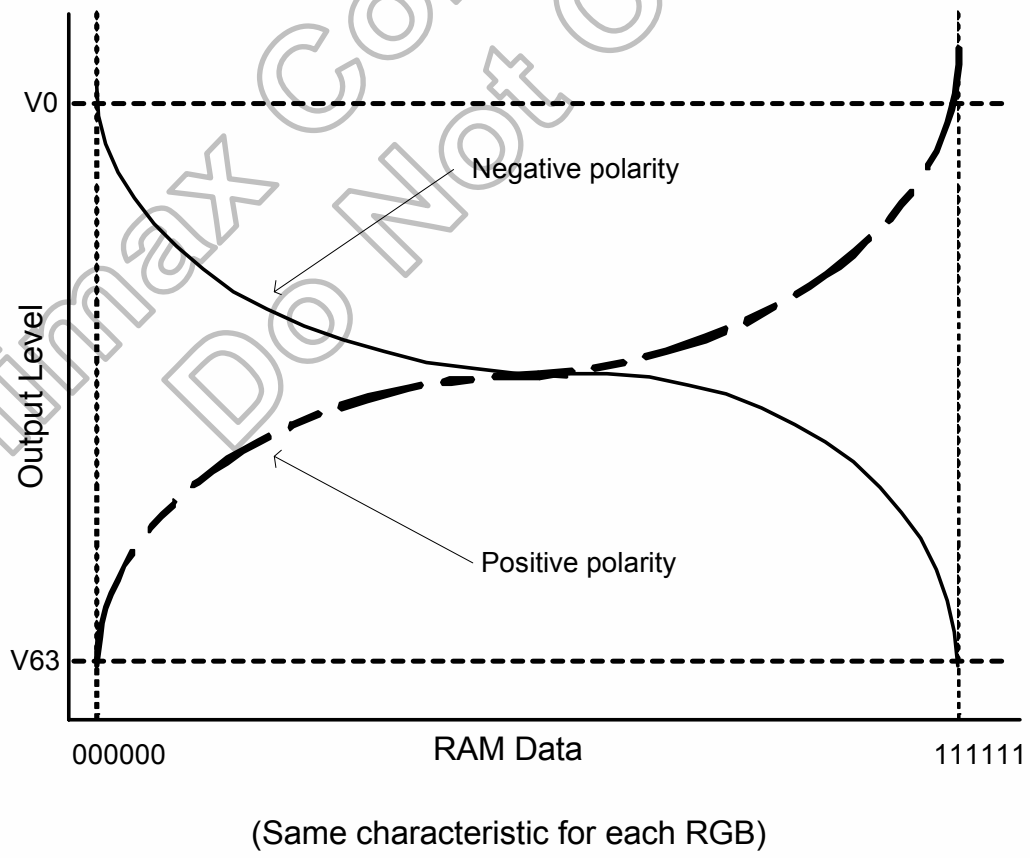

Figure 5. 41 Relationships between GRAM Data and Output Level

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5.9.2 Gray voltage generator for digital gamma correction

The HX8352-A digital gamma correction can reach the independent GAMMA curve of RGB. HX8352-A utilizes LUT to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

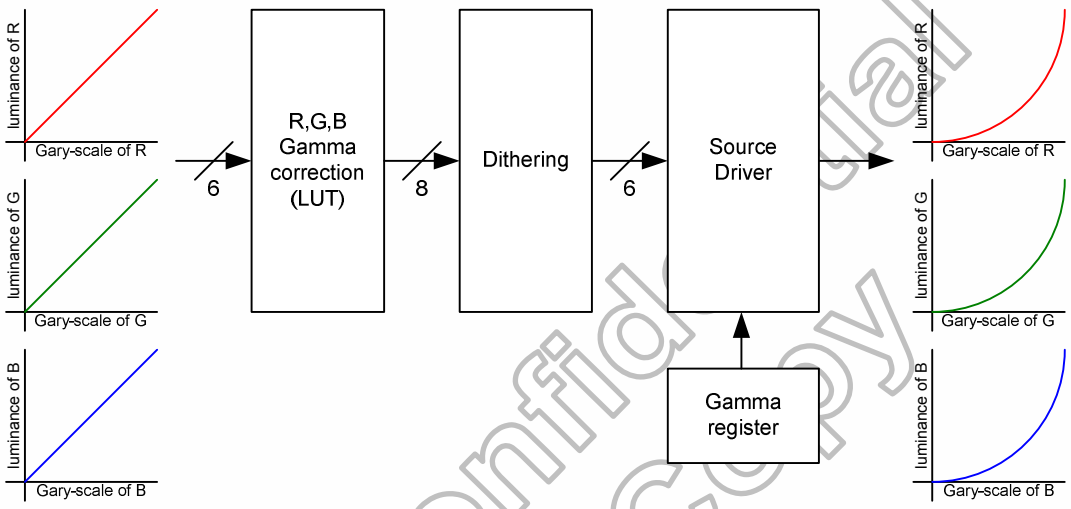

Figure 5. 42 Block Diagram of Digital Gamma Correction

The HX8352-A builds one 192-bytes LUT (Look up table) to transfer every display data of Dithering circuit input and setting by DGC LUT register (R2Fh).

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R input (6 bit)	R output (8bit)	DGC LUT Parameter byte
000000	R_{007} $R_{006}R_{005}$ $R_{004}R_{003}R_{002}R_{001}R_{000}$	1
000001	$R_{017}R_{016}R_{015}R_{014}R_{013}R_{012}R_{011}R_{010}$	2
000010	$R_{027}R_{026}R_{025}R_{024}R_{023}R_{022}R_{021}R_{020}$	3
000011	$R_{037}R_{036}R_{035}R_{034}R_{033}R_{032}R_{031}R_{030}$	4
000100	$R_{047}R_{046}R_{045}R_{044}R_{043}R_{042}R_{041}R_{040}$	5
000101	$R_{057}R_{056}R_{055}R_{054}R_{053}R_{052}R_{051}R_{050}$	6
000110	$R_{067}R_{066}R_{065}R_{064}R_{063}R_{062}R_{061}R_{060}$	7
000111	$R_{077}R_{076}R_{075}R_{074}R_{073}R_{072}R_{071}R_{070}$	8
001000	$R_{087}R_{086}R_{085}R_{084}R_{083}R_{082}R_{081}R_{080}$	9
001001	$R_{097}R_{096}R_{095}R_{094}R_{093}R_{092}R_{091}R_{090}$	10
001010	$R_{107}R_{106}R_{105}R_{104}R_{103}R_{102}R_{101}R_{100}$	11
001011	$R_{117}R_{116}R_{115}R_{114}R_{113}R_{112}R_{111}R_{110}$	12
001100	$R_{127}R_{126}R_{125}R_{124}R_{123}R_{122}R_{121}R_{120}$	13
001101	$R_{137}R_{136}R_{135}R_{134}R_{133}R_{132}R_{131}R_{130}$	14
001110	$R_{147}R_{146}R_{145}R_{144}R_{143}R_{142}R_{141}R_{140}$	15
001111	$R_{157}R_{156}R_{155}R_{154}R_{153}R_{152}R_{151}R_{150}$	16
010000	R_{167} $R_{166}R_{165}$ $R_{164}R_{163}R_{162}R_{161}R_{160}$	17
010001	$R_{177}R_{176}R_{175}R_{174}R_{173}R_{172}R_{171}R_{170}$	18
010010	$R_{187}R_{186}R_{185}R_{184}R_{183}R_{182}R_{181}R_{180}$	19
010011	$R_{197}R_{196}R_{195}R_{194}R_{193}R_{192}R_{191}R_{190}$	20
010100	$R_{207}R_{206}R_{205}R_{204}R_{203}R_{202}R_{201}R_{200}$	21
010101	$R_{217}R_{216}R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$	22
010110	$R_{227}R_{226}R_{225}R_{224}R_{223}R_{222}R_{221}R_{220}$	23
010111	$R_{237}R_{236}R_{235}R_{234}R_{233}R_{232}R_{231}R_{230}$	24
011000	$R_{247}R_{246}R_{245}R_{244}R_{243}R_{242}R_{241}R_{240}$	25
011001	$R_{257}R_{256}R_{255}R_{254}R_{253}R_{252}R_{251}R_{250}$	26
011010	$R_{267}R_{266}R_{265}R_{264}R_{263}R_{262}R_{261}R_{260}$	27
011011	$R_{277}R_{276}R_{275}R_{274}R_{273}R_{272}R_{271}R_{270}$	28
011100	$R_{287}R_{286}R_{285}R_{284}R_{283}R_{282}R_{281}R_{280}$	29
011101	$R_{297}R_{296}R_{295}R_{294}R_{293}R_{292}R_{291}R_{290}$	30
011110	$R_{307}R_{306}R_{305}R_{304}R_{303}R_{302}R_{301}R_{300}$	31
011111	$R_{317}R_{316}R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$	32

Table 5. 20 LUT for Red Color (1)

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R input (6 bit)	R output (8bit)	DGC LUT Parameter byte
100000	R_{327} $R_{326}R_{325}$ $R_{324}R_{323}R_{322}R_{321}R_{320}$	33
100001	$R_{337}R_{336}R_{335}R_{334}R_{333}R_{332}R_{331}R_{330}$	34
100010	$R_{347}R_{346}R_{345}R_{344}R_{343}R_{342}R_{341}R_{340}$	35
100011	$R_{357}R_{356}R_{355}R_{354}R_{353}R_{352}R_{351}R_{350}$	36
100100	$R_{367}R_{366}R_{365}R_{364}R_{363}R_{362}R_{361}R_{360}$	37
100101	$R_{377}R_{376}R_{375}R_{374}R_{373}R_{372}R_{371}R_{370}$	38
100110	$R_{387}R_{386}R_{385}R_{384}R_{383}R_{382}R_{381}R_{380}$	39
100111	$R_{397}R_{396}R_{395}R_{394}R_{393}R_{392}R_{391}R_{390}$	40
101000	$R_{407}R_{406}R_{405}R_{404}R_{403}R_{402}R_{401}R_{400}$	41
101001	$R_{417}R_{416}R_{415}R_{414}R_{413}R_{412}R_{411}R_{410}$	42
101010	$R_{427}R_{426}R_{425}R_{424}R_{423}R_{422}R_{421}R_{420}$	43
101011	$R_{437}R_{436}R_{435}R_{434}R_{433}R_{432}R_{431}R_{430}$	44
101100	$R_{447}R_{446}R_{445}R_{444}R_{443}R_{442}R_{441}R_{440}$	45
101101	$R_{457}R_{456}R_{455}R_{454}R_{453}R_{452}R_{451}R_{450}$	46
101110	$R_{467}R_{466}R_{465}R_{464}R_{463}R_{462}R_{461}R_{460}$	47
101111	$R_{477}R_{476}R_{475}R_{474}R_{473}R_{472}R_{471}R_{470}$	48
110000	R_{487} $R_{486}R_{485}$ $R_{484}R_{483}R_{482}R_{481}R_{480}$	49
110001	$R_{497}R_{496}R_{495}R_{494}R_{493}R_{492}R_{491}R_{490}$	50
110010	$R_{507}R_{506}R_{505}R_{504}R_{503}R_{502}R_{501}R_{500}$	51
110011	$R_{517}R_{516}R_{515}R_{514}R_{513}R_{512}R_{511}R_{510}$	52
110100	$R_{527}R_{526}R_{525}R_{524}R_{523}R_{522}R_{521}R_{520}$	53
110101	$R_{537}R_{536}R_{535}R_{534}R_{533}R_{532}R_{531}R_{530}$	54
110110	$R_{547}R_{546}R_{545}R_{544}R_{543}R_{542}R_{541}R_{540}$	55
110111	$R_{557}R_{556}R_{555}R_{554}R_{553}R_{552}R_{551}R_{550}$	56
111000	$R_{567}R_{566}R_{565}R_{564}R_{563}R_{562}R_{561}R_{560}$	57
111001	$R_{577}R_{576}R_{575}R_{574}R_{573}R_{572}R_{571}R_{570}$	58
111010	$R_{587}R_{586}R_{585}R_{584}R_{583}R_{582}R_{581}R_{580}$	59
111011	$R_{597}R_{596}R_{595}R_{594}R_{593}R_{592}R_{591}R_{590}$	60
111100	$R_{607}R_{606}R_{605}R_{604}R_{603}R_{602}R_{601}R_{600}$	61
111101	$R_{617}R_{616}R_{615}R_{614}R_{613}R_{612}R_{611}R_{610}$	62
111110	$R_{627}R_{626}R_{625}R_{624}R_{623}R_{622}R_{621}R_{620}$	63
111111	$R_{637}R_{636}R_{635}R_{634}R_{633}R_{632}R_{631}R_{630}$	64

Table 5. 21 LUT for Red Color (2)

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G input (6 bit)	G output (8bit)	DGC LUT Parameter byte
000000	G_{007} $G_{006}G_{005}$ $G_{004}G_{003}G_{002}G_{001}G_{000}$	65
000001	$G_{017}G_{016}G_{015}G_{014}G_{013}G_{012}G_{011}G_{010}$	66
000010	$G_{027}G_{026}G_{025}G_{024}G_{023}G_{022}G_{021}G_{020}$	67
000011	$G_{037}G_{036}G_{035}G_{034}G_{033}G_{032}G_{031}G_{030}$	68
000100	$G_{047}G_{046}G_{045}G_{044}G_{043}G_{042}G_{041}G_{040}$	69
000101	$G_{057}G_{056}G_{055}G_{054}G_{053}G_{052}G_{051}G_{050}$	70
000110	$G_{067}G_{066}G_{065}G_{064}G_{063}G_{062}G_{061}G_{060}$	71
000111	$G_{077}G_{076}G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$	72
001000	$G_{087}G_{086}G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$	73
001001	$G_{097}G_{096}G_{095}G_{094}G_{093}G_{092}G_{091}G_{090}$	74
001010	$G_{107}G_{106}G_{105}G_{104}G_{103}G_{102}G_{101}G_{100}$	75
001011	$G_{117}G_{116}G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$	76
001100	$G_{127}G_{126}G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$	77
001101	$G_{137}G_{136}G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$	78
001110	$G_{147}G_{146}G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$	79
001111	$G_{157}G_{156}G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$	80
010000	G_{167} $G_{166}G_{165}$ $G_{164}G_{163}G_{162}G_{161}G_{160}$	81
010001	$G_{177}G_{176}G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$	82
010010	$G_{187}G_{186}G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$	83
010011	$G_{197}G_{196}G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$	84
010100	$G_{207}G_{206}G_{205}G_{204}G_{203}G_{202}G_{201}G_{200}$	85
010101	$G_{217}G_{216}G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	86
010110	$G_{227}G_{226}G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$	87
010111	$G_{237}G_{236}G_{235}G_{234}G_{233}G_{232}G_{231}G_{230}$	88
011000	$G_{247}G_{246}G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	89
011001	$G_{257}G_{256}G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$	90
011010	$G_{267}G_{266}G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$	91
011011	$G_{277}G_{276}G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$	92
011100	$G_{287}G_{286}G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$	93
011101	$G_{297}G_{296}G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$	94
011110	$G_{307}G_{306}G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$	95
011111	$G_{317}G_{316}G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$	96

Table 5. 22 LUT for Green Color (1)

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G input (6 bit)	G output (8bit)	DGC LUT Parameter byte
100000	G_{327} $G_{326}G_{325}$ $G_{324}G_{323}G_{322}G_{321}G_{320}$	97
100001	$G_{337}G_{336}G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	98
100010	$G_{347}G_{346}G_{345}G_{344}G_{343}G_{342}G_{341}G_{340}$	99
100011	$G_{357}G_{356}G_{355}G_{354}G_{353}G_{352}G_{351}G_{350}$	100
100100	$G_{367}G_{366}G_{365}G_{364}G_{363}G_{362}G_{361}G_{360}$	101
100101	$G_{377}G_{376}G_{375}G_{374}G_{373}G_{372}G_{371}G_{370}$	102
100110	$G_{387}G_{386}G_{385}G_{384}G_{383}G_{382}G_{381}G_{380}$	103
100111	$G_{397}G_{396}G_{395}G_{394}G_{393}G_{392}G_{391}G_{390}$	104
101000	$G_{407}G_{406}G_{405}G_{404}G_{403}G_{402}G_{401}G_{400}$	105
101001	$G_{417}G_{416}G_{415}G_{414}G_{413}G_{412}G_{411}G_{410}$	106
101010	$G_{427}G_{426}G_{425}G_{424}G_{423}G_{422}G_{421}G_{420}$	107
101011	$G_{437}G_{436}G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$	108
101100	$G_{447}G_{446}G_{445}G_{444}G_{443}G_{442}G_{441}G_{440}$	109
101101	$G_{457}G_{456}G_{455}G_{454}G_{453}G_{452}G_{451}G_{450}$	110
101110	$G_{467}G_{466}G_{465}G_{464}G_{463}G_{462}G_{461}G_{460}$	111
101111	$G_{477}G_{476}G_{475}G_{474}G_{473}G_{472}G_{471}G_{470}$	112
110000	G_{487} $G_{486}G_{485}$ $G_{484}G_{483}G_{482}G_{481}G_{480}$	113
110001	$G_{497}G_{496}G_{495}G_{494}G_{493}G_{492}G_{491}G_{490}$	114
110010	$G_{507}G_{506}G_{505}G_{504}G_{503}G_{502}G_{501}G_{500}$	115
110011	$G_{517}G_{516}G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$	116
110100	$G_{527}G_{526}G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$	117
110101	$G_{537}G_{536}G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$	118
110110	$G_{547}G_{546}G_{545}G_{544}G_{543}G_{542}G_{541}G_{540}$	119
110111	$G_{557}G_{556}G_{555}G_{554}G_{553}G_{552}G_{551}G_{550}$	120
111000	$G_{567}G_{566}G_{565}G_{564}G_{563}G_{562}G_{561}G_{560}$	121
111001	$G_{577}G_{576}G_{575}G_{574}G_{573}G_{572}G_{571}G_{570}$	122
111010	$G_{587}G_{586}G_{585}G_{584}G_{583}G_{582}G_{581}G_{580}$	123
111011	$G_{597}G_{596}G_{595}G_{594}G_{593}G_{592}G_{591}G_{590}$	124
111100	$G_{607}G_{606}G_{605}G_{604}G_{603}G_{602}G_{601}G_{600}$	125
111101	$G_{617}G_{616}G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$	126
111110	$G_{627}G_{626}G_{625}G_{624}G_{623}G_{622}G_{621}G_{620}$	127
111111	$G_{637}G_{636}G_{635}G_{634}G_{633}G_{632}G_{631}G_{630}$	128

Table 5. 23 LUT for Green Color (2)

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B input (6 bit)	B output (8bit)	DGC LUT Parameter byte
000000	B_{007} $B_{006}B_{005}$ $B_{004}B_{003}B_{002}B_{001}B_{000}$	129
000001	$B_{017}B_{016}B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$	130
000010	$B_{027}B_{026}B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$	131
000011	$B_{037}B_{036}B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$	132
000100	$B_{047}B_{046}B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$	133
000101	$B_{057}B_{056}B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$	134
000110	$B_{067}B_{066}B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$	135
000111	$B_{077}B_{076}B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$	136
001000	$B_{087}B_{086}B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$	137
001001	$B_{097}B_{096}B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$	138
001010	$B_{107}B_{106}B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$	139
001011	$B_{117}B_{116}B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$	140
001100	$B_{127}B_{126}B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$	141
001101	$B_{137}B_{136}B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$	142
001110	$B_{147}B_{146}B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$	143
001111	$B_{157}B_{156}B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$	144
010000	B_{167} $B_{166}B_{165}$ $B_{164}B_{163}B_{162}B_{161}B_{160}$	145
010001	$B_{177}B_{176}B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$	146
010010	$B_{187}B_{186}B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$	147
010011	$B_{197}B_{196}B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$	148
010100	$B_{207}B_{206}B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$	149
010101	$B_{217}B_{216}B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$	150
010110	$B_{227}B_{226}B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$	151
010111	$B_{237}B_{236}B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$	152
011000	$B_{247}B_{246}B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$	153
011001	$B_{257}B_{256}B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$	154
011010	$B_{267}B_{266}B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$	155
011011	$B_{277}B_{276}B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$	156
011100	$B_{287}B_{286}B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$	157
011101	$B_{297}B_{296}B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$	158
011110	$B_{307}B_{306}B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$	159
011111	$B_{317}B_{316}B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$	160

Table 5. 24 LUT for Blue Color (1)

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B input (6 bit)	B output (8bit)	DGC LUT Parameter byte
100000	B_{327} $B_{326}B_{325}$ $B_{324}B_{323}B_{322}B_{321}B_{320}$	161
100001	$B_{337}B_{336}B_{335}B_{334}B_{333}B_{332}B_{331}B_{330}$	162
100010	$B_{347}B_{346}B_{345}B_{344}B_{343}B_{342}B_{341}B_{340}$	163
100011	$B_{357}B_{356}B_{355}B_{354}B_{353}B_{352}B_{351}B_{350}$	164
100100	$B_{367}B_{366}B_{365}B_{364}B_{363}B_{362}B_{361}B_{360}$	165
100101	$B_{377}B_{376}B_{375}B_{374}B_{373}B_{372}B_{371}B_{370}$	166
100110	$B_{387}B_{386}B_{385}B_{384}B_{383}B_{382}B_{381}B_{380}$	167
100111	$B_{397}B_{396}B_{395}B_{394}B_{393}B_{392}B_{391}B_{390}$	168
101000	$B_{407}B_{406}B_{405}B_{404}B_{403}B_{402}B_{401}B_{400}$	169
101001	$B_{417}B_{416}B_{415}B_{414}B_{413}B_{412}B_{411}B_{410}$	170
101010	$B_{427}B_{426}B_{425}B_{424}B_{423}B_{422}B_{421}B_{420}$	171
101011	$B_{437}B_{436}B_{435}B_{434}B_{433}B_{432}B_{431}B_{430}$	172
101100	$B_{447}B_{446}B_{445}B_{444}B_{443}B_{442}B_{441}B_{440}$	173
101101	$B_{457}B_{456}B_{455}B_{454}B_{453}B_{452}B_{451}B_{450}$	174
101110	$B_{467}B_{466}B_{465}B_{464}B_{463}B_{462}B_{461}B_{460}$	175
101111	$B_{477}B_{476}B_{475}B_{474}B_{473}B_{472}B_{471}B_{470}$	176
110000	B_{487} $B_{486}B_{485}$ $B_{484}B_{483}B_{482}B_{481}B_{480}$	177
110001	$B_{497}B_{496}B_{495}B_{494}B_{493}B_{492}B_{491}B_{490}$	178
110010	$B_{507}B_{506}B_{505}B_{504}B_{503}B_{502}B_{501}B_{500}$	179
110011	$B_{517}B_{516}B_{515}B_{514}B_{513}B_{512}B_{511}B_{510}$	180
110100	$B_{527}B_{526}B_{525}B_{524}B_{523}B_{522}B_{521}B_{520}$	181
110101	$B_{537}B_{536}B_{535}B_{534}B_{533}B_{532}B_{531}B_{530}$	182
110110	$B_{547}B_{546}B_{545}B_{544}B_{543}B_{542}B_{541}B_{540}$	183
110111	$B_{557}B_{556}B_{555}B_{554}B_{553}B_{552}B_{551}B_{550}$	184
111000	$B_{567}B_{566}B_{565}B_{564}B_{563}B_{562}B_{561}B_{560}$	185
111001	$B_{577}B_{576}B_{575}B_{574}B_{573}B_{572}B_{571}B_{570}$	186
111010	$B_{587}B_{586}B_{585}B_{584}B_{583}B_{582}B_{581}B_{580}$	187
111011	$B_{597}B_{596}B_{595}B_{594}B_{593}B_{592}B_{591}B_{590}$	188
111100	$B_{607}B_{606}B_{605}B_{604}B_{603}B_{602}B_{601}B_{600}$	189
111101	$B_{617}B_{616}B_{615}B_{614}B_{613}B_{612}B_{611}B_{610}$	190
111110	$B_{627}B_{626}B_{625}B_{624}B_{623}B_{622}B_{621}B_{620}$	191
111111	$B_{637}B_{636}B_{635}B_{634}B_{633}B_{632}B_{631}B_{630}$	192

Table 5. 25 LUT for Blue Color (2)

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5.10 Scan mode setting

The HX8352-A can set internal register SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8352-A.

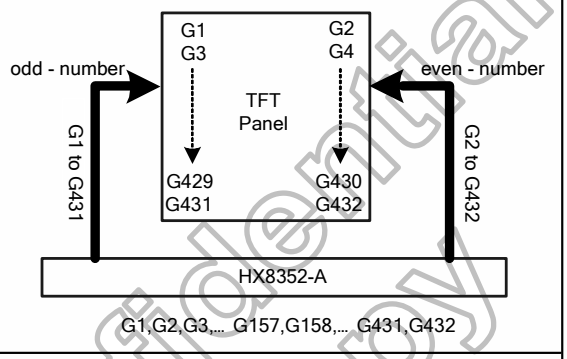
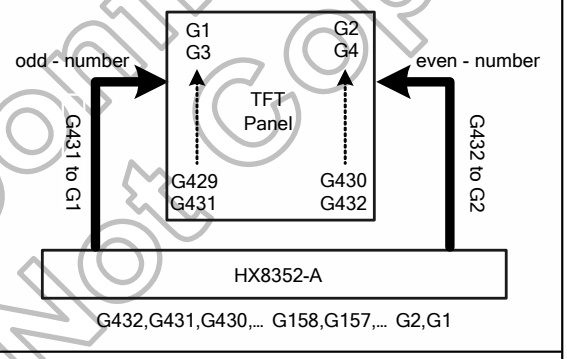
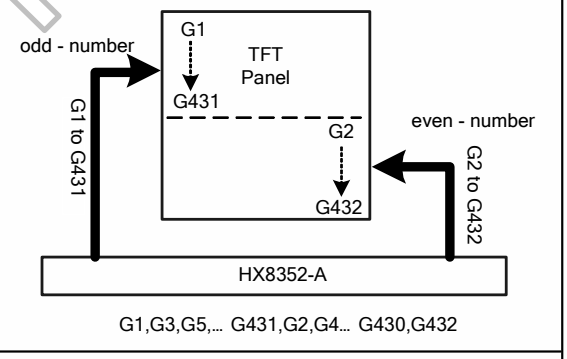
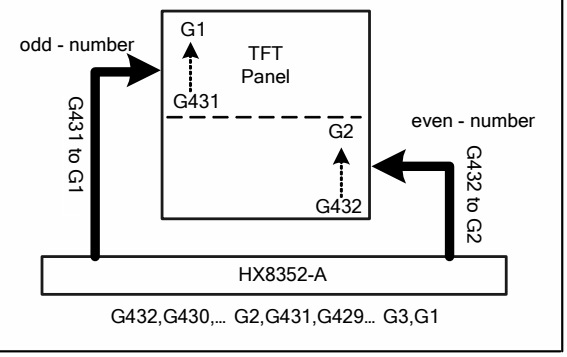
SM	GS	Scan direction
0	0	
0	1	
1	0	
1	1	

Figure 5. 43 Scan Function (240RGB x 432 Dot)

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5.11 Register setting flow

The following are the sequences of register setting flow that applied to the HX8352-A driving the TFT display, when operate in Register-Content interface mode.

Display on/off set flow

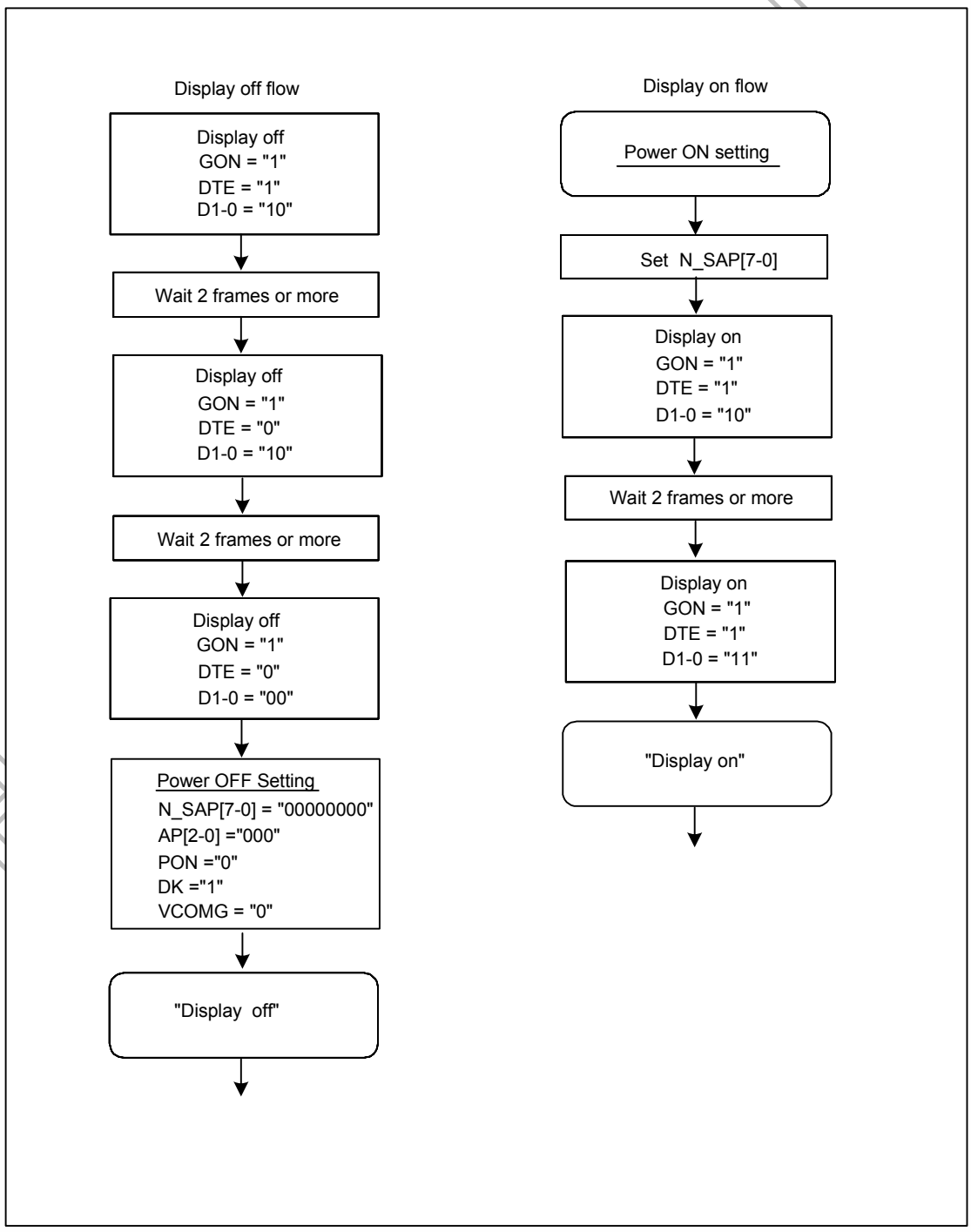

Figure 5. 44 Display On/Off Set Sequence

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Standby mode set flow

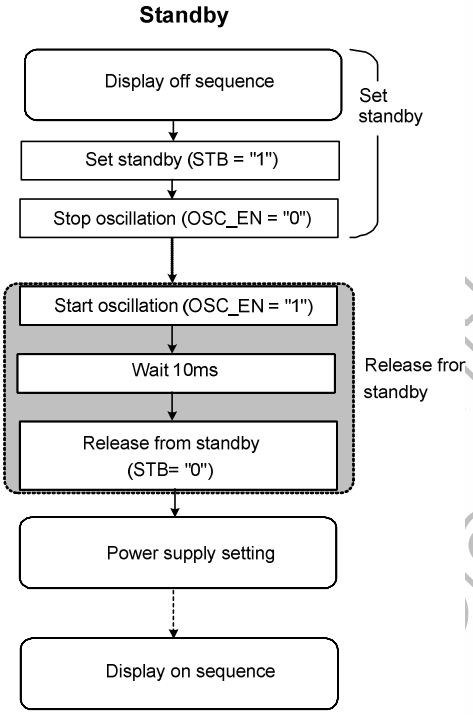

Figure 5. 45 Standby Mode Setting Sequence

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5.12 Power supply setting

The power supply setting sequence of the HX8352-A is shown as blew.

Power supply setting flow

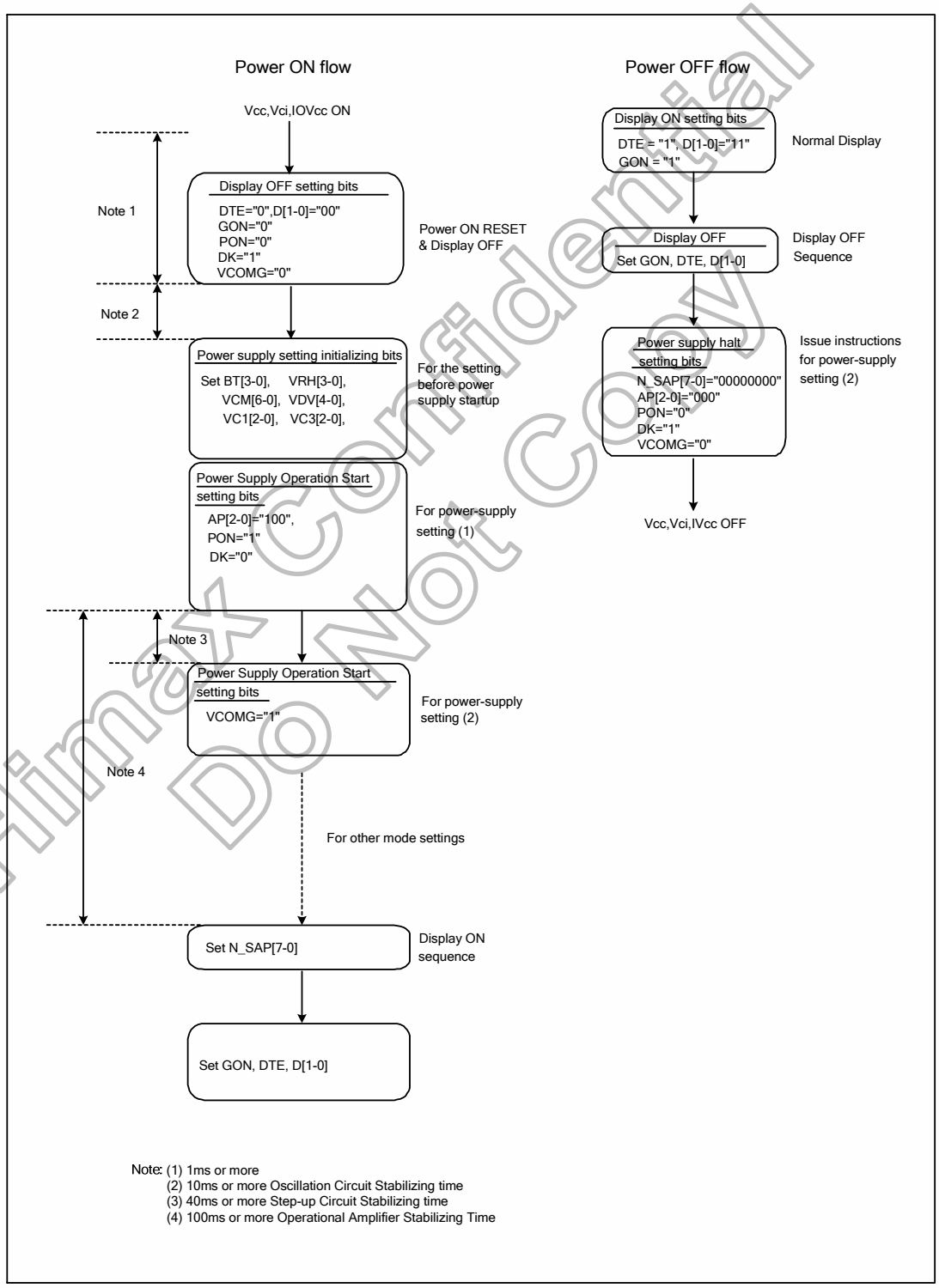

Figure 5. 46 Power Supply Setting Flow

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5.13 OTP programming

OTP_INDEX	D7	D6	D5	D4	D3	D2	D1	D0
00h	Himax Internal use							
01h	(no use)			Himax Internal use				
02h	Himax Internal use							
03h	(no use)			Himax Internal use				
04h	Himax Internal use							
05h	(no use)			Himax Internal use				
06h	Himax Internal use							
07h	(no use)			Himax Internal use				
08h	Himax Internal use							
09h	Himax Internal use							
0Ah	Himax Internal use							
0Bh	(no use)							
0Ch	(no use)				Himax Internal use			
0Dh	Himax Internal use				Himax Internal use			(no use)
0Eh	Himax Internal use							
0Fh	NVALID1	(no use)			Himax Internal use			
10h	(no use)				Himax Internal use			
11h	(no use)			VDV[4:0]				
12h	NVALID2	VCM[6:0]						
13h	(no use)			Himax Internal use				
14h	(no use)	Himax Internal use						
15h	(no use)	Himax Internal use						
16h	(no use)	Himax Internal use						
17h	(no use)	Himax Internal use						
18h	(no use)	Himax Internal use						
19h	(no use)	Himax Internal use						
1Ah	(no use)	Himax Internal use						
1Bh	(no use)	Himax Internal use						
1Ch	(no use)	Himax Internal use						
1Dh	(no use)	Himax Internal use						
1Eh	(no use)	Himax Internal use						
1Fh	(no use)	Himax Internal use						
20h	(no use)	Himax Internal use						
21h	(no use)	Himax Internal use						
22h	(no use)	Himax Internal use						
23h	(no use)	Himax Internal use						
24h	(no use)	Himax Internal use						
25h	(no use)	Himax Internal use						
26h	(no use)	Himax Internal use						
27h	(no use)	Himax Internal use						
28h	(no use)	Himax Internal use						
29h	(no use)	Himax Internal use						
2Ah	(no use)	Himax Internal use						
2Bh	(no use)	Himax Internal use						
2Ch	(no use)	Himax Internal use						
2Dh	(no use)	Himax Internal use						
2Eh	(no use)	Himax Internal use						
2Fh	(no use)	Himax Internal use						
30h	Himax Internal use							
31h	NVALID4	Himax Internal use						
32h	Himax Internal use							
33h	NVALID3	(no use)						Internal use
34h	(no use)	Himax Internal use			(no use)			
35h	(no use)			VDV[4:0]				
36h	NVALID5	VCM[6:0]						
37h	(no use)			VDV[4:0]				
38h	NVALID6	VCM[6:0]						

Note: NVALID1~6 are control differential banks.
(1) NVALID1: Control Bank1 (00h ~ 10h).
(2) NVALID2: Control Bank1 (11h ~ 12h).
(3) NVALID3: Control Bank1 (13h ~ 2Fh, 33h~34h).
(4) NVALID4: Control Bank1 (30h ~ 32h).
(5) NVALID5: Control Bank1 (35h ~ 36h).
(6) NVALID6: Control Bank1 (37h ~ 38h).
NVALIDx: 1 -> Not reload data of OTP to register; 0 -> Need reload data of OTP to register.

Table 5. 26 OTP Memory Table

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Programming flow

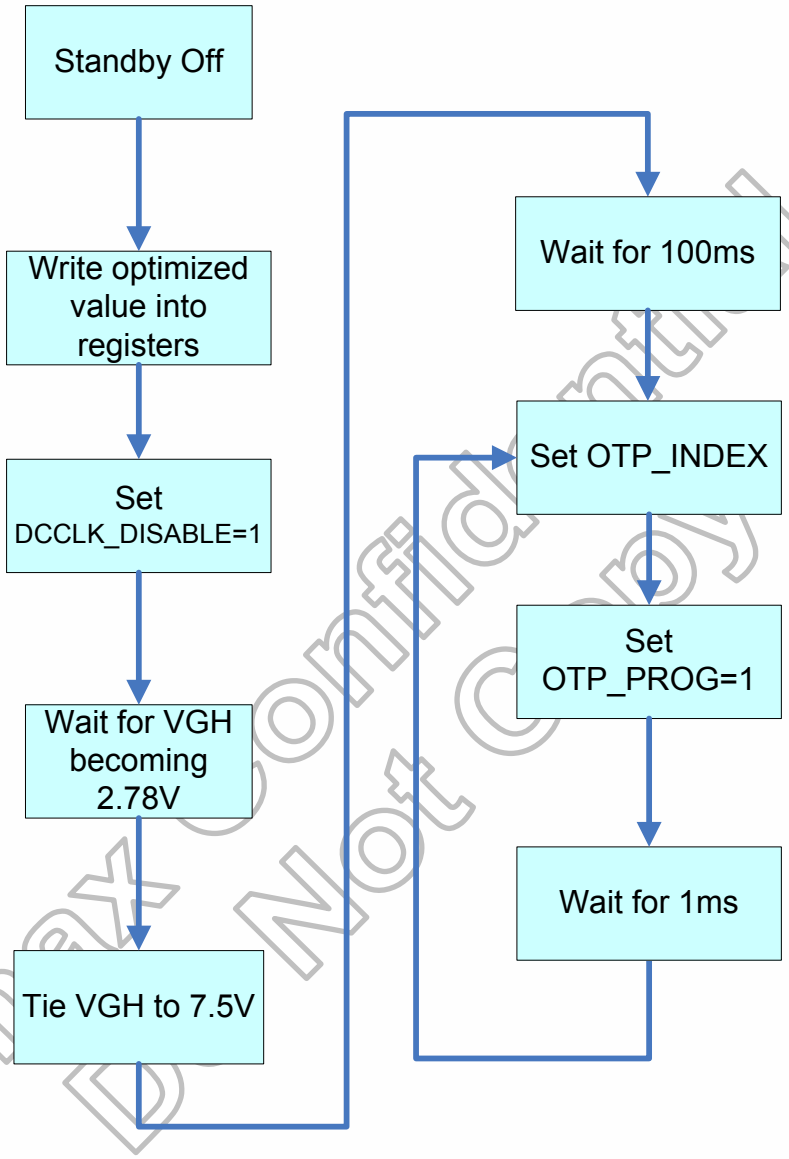
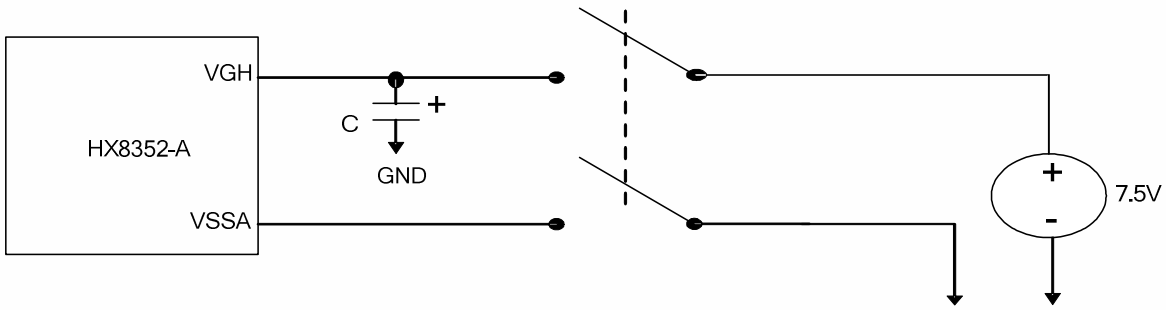


Figure 5. 47 OTP Programming Flow

Programming circuitry



Note: (1)Connect external power at Step 7
(2) C=1uF(built-In or the module)

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Programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and reset the module</td></tr>
<tr><td>2</td><td>Set OTP_LOAD_DISABLE=1, disable the auto-loading function.</td></tr>
<tr><td>3</td><td>OSC_EN=1, STB=0</td></tr>
<tr><td>4</td><td>Wait 120ms</td></tr>
<tr><td>5</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td>OSC Control1 (17h)</td><td>RADJ[3:0]</td><td>The division ratio of clocks in display mode</td></tr>
<tr><td>IP control (5Ah)</td><td>DGC_EN</td><td>DGC function Disable/Enable</td></tr>
<tr><td>VCOM Control (1Fh)</td><td>VCM[6:0]</td><td>VcomH voltage (High level voltage of VCOM)</td></tr>
<tr><td>Power Control1 (1Eh)</td><td>VDV[4:0]</td><td>Vcom amplitude (VcomL = VcomH – Vcom amplitude, VcomL ≥ VCL+0.5V)</td></tr>
<tr><td>PANEL Control Register (R55h)</td><td>BGR_PANEL, SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL</td><td>PANEL Control</td></tr>
</table>
Note: ID1~ID3 are don’t care in Register-Content Interface mode.</td></tr>
<tr><td>6</td><td>Set OTP_ DCCLK_DISABLE=1, disable internal pumping clock.</td></tr>
<tr><td>7</td><td>Wait 500ms for power down</td></tr>
<tr><td>8</td><td>Connect external power 7.5V to VGH pin</td></tr>
<tr><td>9</td><td>Wait 100ms for VGH stable</td></tr>
<tr><td>10</td><td>Specify OTP_index
<table>
<tr><th>OTP_index</th><th>Parameter</th></tr>
<tr><td>0x10h</td><td>RADJ[3:0]</td></tr>
<tr><td>0x11h</td><td>VDV[4:0]</td></tr>
<tr><td>0x12h</td><td>VCM[6:0</td></tr>
<tr><td>0x13h</td><td>BGR_PANEL, SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL</td></tr>
<tr><td>0x33h</td><td>DGC_EN</td></tr>
</table></td></tr>
<tr><td>11</td><td>Set OTP_Mask=0x00h, programming the entire bit of one parameter.</td></tr>
<tr><td>12</td><td>Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.</td></tr>
<tr><td>13</td><td>Wait 1 ms</td></tr>
<tr><td>14</td><td>Complete programming one parameter to OTP. If continue to programming other parameter, set OTP_PROG=0 before return to step (9). Otherwise, power off the module and remove the external power on VGH pin.</td></tr>
</table>

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5.14 Free running mode specification

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FR-mode). For burn-in, it is sufficient that the display is powered up with a plane saturated black or saturated white pattern. Black should be used for burn-in, since this result in a larger pixel voltage. White is used to verify if the free running mode is properly functioning. Please note that the black and the white pattern are reversed in case of a normally black display.

Parameter	Symbol	Description
Power supply pins	IOVCC, VCI, VCC	All power supply pins
Free running mode	BURN	BURN=1, FR-mode is enabled.
Reset	NRESET	Active low pulse in order to start the FR-mode.
Chip select(1)	NCS	This pin will be left open during FRM mode.
Data enable(1)	ENABLE	This pin will be left open during FRM mode.
Reads/not write(1)	NRD_E, WR_RNW	This pin will be left open during FRM mode.
Data/not command(1)	DNC_SCL	This pin will be left open during FRM mode.
Horizontal sync(1)	HSYNC	This pin will be left open during FRM mode.
Vertical sync(1)	VSYNC	This pin will be left open during FRM mode.
Data clock	DOTCLK	This pin will be left open during FRM mode.
CPU I/F Data(1)	DB[0..17]	This pin will be left open during FRM mode.
SPI I/F Data(1)	SDI, SDO	This pin will be left open during FRM mode.

Note: (1) The BURN-pin has a pull down resistor inside the driver IC, because this pin will be left open during the normal operation in the application. The BURN-pin must be logical high for longer than 5ms before the driver IC will switch to the FR-mode in order to avoid disturbances during normal operation.
(2) As a general rule, all control pins of the interfaces like chip-select, data-enable, etc must be disabled, all mode select pins like data-not-command, interface-select etc and all data-bus pins must be set to eider logic high or logic low during the FR-mode.

Table 5. 27 Pin Information of Free Running Mode

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Power-on sequence

The FR-mode starts automatically after the power supply is switched on and a reset pulse is applied to the Reset-pin, if the BURN pin is set to logical high. In case of separate supply pins for the analogue supply and digital supply, both supply pins will be connected together, if it is supported by the driver specification. Otherwise, each supply voltage will be switched on separately according to the requested power-on sequence. The BURN and all other digital I/F pins, which will be set to logic high during the free running mode, can be switched to logic high together with the digital supply pin. The FR-mode will be restarted if the reset pulse is applied a second time. The OTP starts to load when Reset leaves low to high.

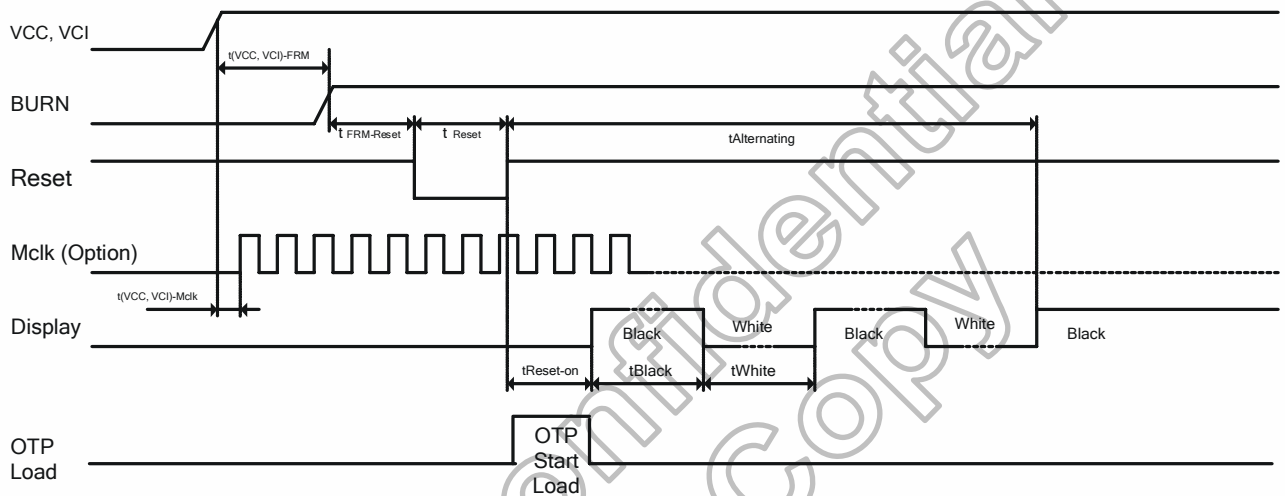

Figure 5. 48 Power On Sequence of FR-mode (for Normally–White Panel)

Power off sequence

The power supply can be switched off any time.

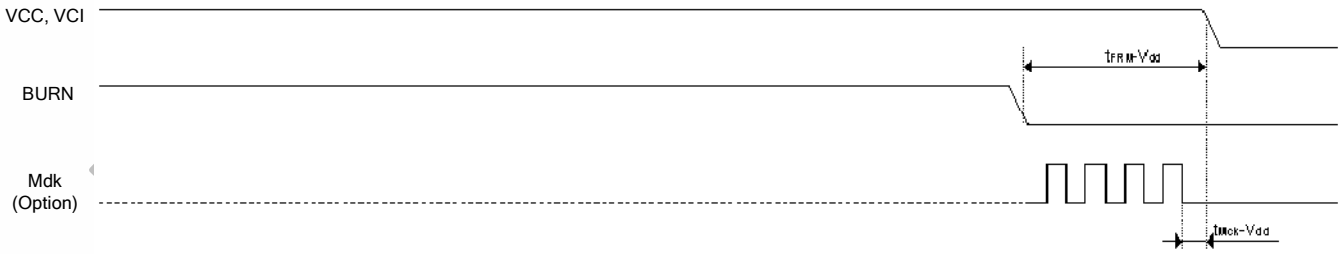

Figure 5. 49 Power Off Sequence of FR-mode

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Free running mode display

The display will show an alternating black and white picture for about the first 5 minutes. The black to white ratio shell be 50%. The time of the black and white pattern shell is around 1 second in order to avoid a too long waiting time to verify that the FR-mode is functioning properly. The display is switched to a static black pattern after the alternating mode is finished. Thus, most efficient burn-in stress is ensured. The display shall work in idle-mode. There is no special restriction for the frame frequency. It can be between 5 and 100Hz. The frame frequency will be set according to the parameter in the OTP.

Alternating Black and White Pattern	$t_{Alternating}$	-	5	-	min
Master Clock Frequency	f_{Mclk}	-	-	10	MHz

Table 5. 28 Frequency Definition of Free Running Mode Display

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6. Command

6.1 Command set

Address	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
8'h00	Product ID	R	0	1	0	1	0	0	1	0
8'h01	Display mode	R/W	0	0	0	0	IDMON(0)	INVON (0)	NORON(1)	PTLON(0)
8'h02	Column Address Start(1)	R/W	SC[15:8] (8'b0)							
8'h03	Column Address Start(2)	R/W	SC[7:0] (8'b0)							
8'h04	Column Address End(1)	R/W	EC[15:8] (8'b0000_0000)							
8'h05	Column Address End(2)	R/W	EC[7:0] (8'b1110_1111)							
8'h06	Row Address Start(1)	R/W	SP[15:8] (8'b0)							
8'h07	Row Address Start(2)	R/W	SP[7:0] (8'b0)							
8'h08	Row Address End(1)	R/W	EP[15:8] (8'b0000_0001)							
8'h09	Row Address End(2)	R/W	EP[7:0] (8'b1010_1111)							
8'h0a	Partial Area Start Row(1)	R/W	PSL[15:8] (8'b0)							
8'h0b	Partial Area Start Row(2)	R/W	PSL[7:0] (8'b0)							
8'h0c	Partial Area End Row(1)	R/W	PEL[15:8] (8'b0000_0001)							
8'h0d	Partial Area End Row(2)	R/W	PEL[7:0] (8'b1010_1111)							
8'h0e	Vertical Scroll Top Fixed Area(1)	R/W	TFA[15:8] (8'b0)							
8'h0f	Vertical Scroll Top Fixed Area(2)	R/W	TFA[7:0] (8'b0)							
8'h10	Vertical Scroll Height Area(1)	R/W	VSA[15:8] (8'b0000_0001)							
8'h11	Vertical Scroll Height Area(2)	R/W	VSA[7:0] (8'b1011_0000)							
8'h12	Vertical Scroll Button Fixed(1)	R/W	BFA[15:8] (8'b0)							
8'h13	Vertical Scroll Button Fixed(2)	R/W	BFA[7:0] (8'b0)							
8'h14	Vertical Scroll Start Address(1)	R/W	VSP[15:8] (8b'0)							
8'h15	Vertical Scroll Start Address(2)	R/W	VSP[7:0] (8b'0)							
8'h16	Memory Access Control	R/W	MY(0)	MX(0)	MV(0)	GS(0)	BGR(0)	SS(0)	SRL_EN[0]	SM[0]
8'h17	OSC Control 1	R/W	RADJ[3:0](1111)							OSC_EN[0]
8'h18	OSC Control 2	R/W	0	UADJ[2:0](011)			CADJ[3:0](1000)			
8'h19	Power Control 1	R/W	GASENB(0)	0	0	PON (0)	DK (1)	XDK[0]	VL_TRI[0]	STB[1]
8'h1a	Power Control 2	R/W	0	VC3[2:0] (000)			0	VC1[2:0] (101)		
8'h1b	Power Control 3	R/W	BT[3:0] (0100)				0	0	AP[1:0] (00)	
8'h1c	Power Control 4	R/W	0	0	0	0	VRH[3:0] (1101)			
8'h1d	Power Control 5	R/W	0	0	0	BGP[3:0] (1000)				
8'h1e	Power Control 6	R/W	0	0	VCOMG (0)	VDV[4:0] (1_0000)				
8'h1f	VCOM Control	R/W	0	VCM[6:0](101_0101)						
8'h22	Data read/write	R/W	SRAM Write							
8'h23	Display Control 1	R/W	0	0	0	0	0	0	TEMODE(0)	TEON(0)
8'h24	Display Control 2	R/W	PT[1:0] (10)		GON (1)	DTE (0)	D[1:0] (00)		0	0
8'h25	Display Control 3	R/W	N_FP[7:0] (8'h02)							
8'h26	Display Control 4	R/W	P_FP[7:0] (8'h02)							
8'h27	Display Control 5	R/W	I_FP[7:0] (8'h02)							
8'h28	Display Control 6	R/W	N_BP[7:0] (8'h02)							
8'h29	Display Control 7	R/W	P_BP[7:0] (8'h02)							
8'h2a	Display Control 8	R/W	I_BP[7:0] (8'h02)							
8'h2b	Cycle Control 1	R/W	N_DC[7:0] (1011_1110)							
8'h2c	Cycle Control 2	R/W	P_DC[7:0] (1011_1110)							
8'h2d	Cycle Control 3	R/W	I_DC[7:0] (1011_1110)							
8'h2e	Cycle Control 4	R/W	FS1[1:0] (01)		FS0[1:0] (00)		I_RTN[3:0] (1000)			
8'h2f	Cycle Control 5	R/W	PI_RTN[3:0] (0000)				N_RTN[3:0] (0000)			
8'h30	Cycle Control 6	R/W	0	0	DIV_I[1:0](00)		0	0	0	I_NW(0)
8'h31	Cycle Control 7	R/W	0	0	DIV_N[1:0](00)		0	0	0	N_NW](1)
8'h32	Cycle Control 8	R/W	0	0	DIV_P[1:0](00)		0	0	0	P_NW(1)
8'h34	Cycle Control 10	R/W	EQS[7:0](0011_1000)							
8'h35	Cycle Control 11	R/W	EQP[7:0](0011_1000)							
8'h36	Cycle Control 12	R/W			PTG[1:0](10)		ISC[3:0] (0001)			
8'h37	Cycle Control 13	R/W	SON[7:0](8'b0011_1000)							
8'h38	Cycle Control 14	R/W	GDON[7:0] (8'b0000_0100)							
8'h39	Cycle Control 15	R/W	GDOF[7:0] (8'b1111_0110)							
8'h3a	Interface Control 1	R/W	CSEL[2:0](110)			0	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)
8'h3c	Source Control 1	R/W	N_SAP[7:0](1100_0000)							
8'h3d	Source Control 2	R/W	I_SAP[7:0](0011_1111)							
8'h3e	Gamma Control 1	R/W	CP1[2:0](000)	CP1[2:0](000)			CP1[2:0](000)	CP1[2:0](000)		
8'h3f	Gamma Control 2	R/W	CN1[2:0](000)	CN1[2:0](000)			CN1[2:0](000)	CN1[2:0](000)		
8'h40	Gamma Control 3	R/W	NP1[2:0](000)	NP1[2:0](000)			NP1[2:0](000)	NP1[2:0](000)		
8'h41	Gamma Control 4	R/W	NP3[2:0](000)	NP3[2:0](000)			NP3[2:0](000)	NP3[2:0](000)		

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Address	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
8'h42	Gamma Control 5	R/W	NP5[2:0](000)	NP5[2:0](000)			NP5[2:0](000)	NP5[2:0](000)		
8'h43	Gamma Control 6	R/W	NN1[2:0](000)	NN1[2:0](000)			NN1[2:0](000)	NN1[2:0](000)		
8'h44	Gamma Control 7	R/W	NN3[2:0](000)	NN3[2:0](000)			NN3[2:0](000)	NN3[2:0](000)		
8'h45	Gamma Control 8	R/W	NN5[2:0](000)	NN5[2:0](000)			NN5[2:0](000)	NN5[2:0](000)		
8'h46	Gamma Control 9	R/W	CGMP1[1:0](00)		CGMP1[1:0](00)		CGMP1[1:0](00)			
8'h47	Gamma Control 10	R/W	CGMP2	CGMP2	CGMP2	CGMP2				
8'h48	Gamma Control 11	R/W	CGMN1[1:0](00)		CGMN1[1:0](00)		CGMN1[1:0](00)			
8'h49	Gamma Control 12	R/W	CGMN2	CGMN2	CGMN2	CGMN2				
8'h55	PANEL Control	R/W	0	0	0	SM_PANEL (0)	SS_PANEL(0)	GS_PANEL(0)	REV_PANEL(0)	BGR_PANEL(0)
8'h56	OTP 1	R/W	OTP_INDEX[7:0] (8'b1111_1111)							
8'h57	OTP 2	R/W	OTP_MASK[7:0] (8'b0)							
8'h58	OTP 3	R/W	DCCLK_DISABLE (0)	DCCLK_DISABLE (0)	DCCLK_DISABLE (0)	DCCLK_DISABLE (0)	OTP_PTM (0)	0	VPP_SEL (0)	OTP_PROG (0)
8'h59	OTP 4	R	OTP_DATA[7:0]							
8'h5a	IP Control	R/W	0	0	0	0	0	0	0	DGC_EN(0)
8'h5c	DGC LUT WRITE	R/W	LUT[7:0](8'b0)							
8'h5d	DATA Control	R/W	0	0	0	0	DFM[1:0](00)		TRI[1:0](00)	
8'h83	Test Mode	R/W	0	0	0	0	0	0	TEST_Mode	0
8'h85	VDDD control	R/W	0	0	0	0	0	VDC_SEL[2:0] (101)		
8'h8A	Powr driving Control	R/W	0	0	0	0	0	PTBA[2:0] (110)		
8'h8B	VGS_RES control 1	R/W	0	0	0	0	0	0	0	RES_VGS1
8'h8C	VGS_RES control 2	R/W	RES_VGS0	0	0	1	0	0	1	1
8'h91	PWM Control 3	R/W	0	0	0	0	0	0	0	SYNC
8'h95	PWM Control 1	R/W	DBV[7:0]							
8'h96	PWM Control 2	R/W	0	0	BCTRL	0	0	BL	0	0
8'h97	PWM Control 3	R/W	0	0	0	0	0	0	C1	C0
8'h6B	CABC Period Control 1	R/W	1	1	1	0	1	SEL_PWMCLK[2:0] (3'b000)		
8'h6C	CABC Period Control 2	R/W	PWM_PERIOD (8'b0101_0100)							
8'h6F	CABC Gain1	R/W	0	BGG0(6:0) (7'b100_0000)						
8'h70	CABC Gain2	R/W	0	BGG1(6:0) (7'b011_0000)						
8'h71	CABC Gain3	R/W	0	BGG2(6:0) (7'b010_1010)						
8'h72	CABC Gain4	R/W	0	BGG3(6:0) (7'b010_1000)						
8'h73	CABC Gain5	R/W	0	BGG4(6:0) (7'b010_0110)						
8'h74	CABC Gain6	R/W	0	BGG5(6:0) (7'b010_0100)						
8'h75	CABC Gain7	R/W	0	BGG6(6:0) (7'b010_0010)						
8'h76	CABC Gain8	R/W	0	BGG7(6:0) (7'b010_0001)						
8'h77	CABC Gain9	R/W	0	BGG8(6:0) (7'b000_0010)						

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6.2 Index register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 6. 1 Index Register

Index register (IR) specifies Index of the register from R00h to RFFh. It sets the register number (ID7-0) in the range from 000000b to 1111111b in binary form.

6.3 Producet ID register (R00h)

R	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	*	*	*	*	*	*	*	*	0	1	0	1	0	0	1	0

Figure 6. 2 Product ID Register (R00h)

Product ID: 0x52h

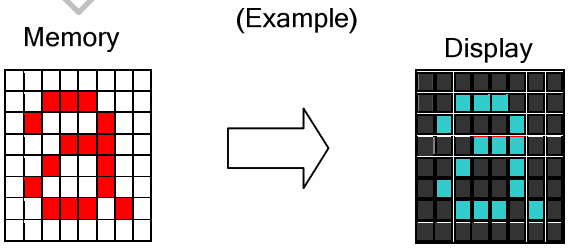
6.4 Display mode control register (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	IDMON (0)	INVON (1)	NORON (1)	PTLON (0)
R	1	*	*	*	*	*	*	*	*	*	*	*	*	IDMON (0)	INVON (1)	NORON (1)	PTLON (0)

Figure 6. 3 Display Mode Control Register (R01h)

IDMON:
This command is used for turning on/off IDLE (8-color display) mode by setting IDMON=1/0.
Note: IDLE ON do not support Digital Gamma used.

INVON:
This command is used to enter into display inversion mode by setting INVON=1. Vise versa, it recovers from display inversion mode by setting INVON=0. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.



NORON:
This command is used for turning on/off NORMAL mode by setting NORON=1/0.

PTLON:
This command is used for turning on/off PARTIAL mode by setting PTLON=1/0.

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6.5 Column address start register (R02~03h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 6. 4 Column Address Start Register Upper Byte (R02h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 6. 5 Column Address Start Register Low Byte (R03h)

6.6 Column address end register (R04~05h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 6. 6 Column Address End Register Upper Byte (R04h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 6. 7 Column Address End Register Low Byte (R05h)

6.7 Row address start register (R06~07h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 6. 8 Row Address Start Register Upper Byte (R06h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 6. 9 Row Address Start Register Low Byte (R07h)

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6.8 Row address end register (R08~09h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 6. 10 Row Address End Register Upper Byte (R08h)

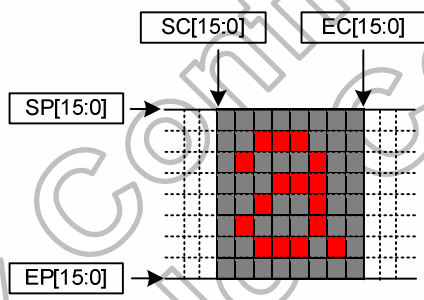
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 6. 11 Row Address End Register Low Byte (R09h)

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. These commands make no change on the other driver status. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.

Note: When one of R02h~R09h write into the IC, then IC will updated whole related register again.

(Example)



6.9 Partial area start row register (R0A~0Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 6. 12 Partial Area Start Row Register Upper Byte (R0Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 6. 13 Partial Area Start Row Register Low Byte (R0Bh)

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6.10 Partial area end row register (R0C~0Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

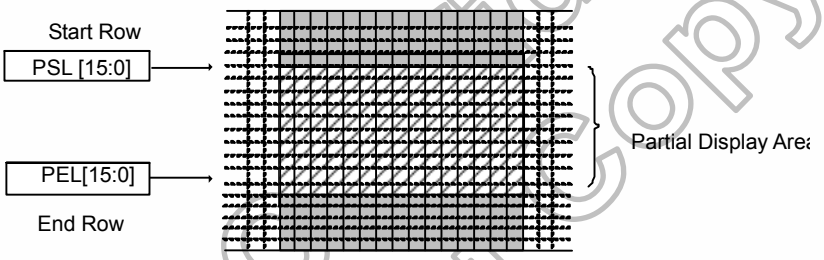
Figure 6. 14 Partial Area End Row Register Upper Byte (R0Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

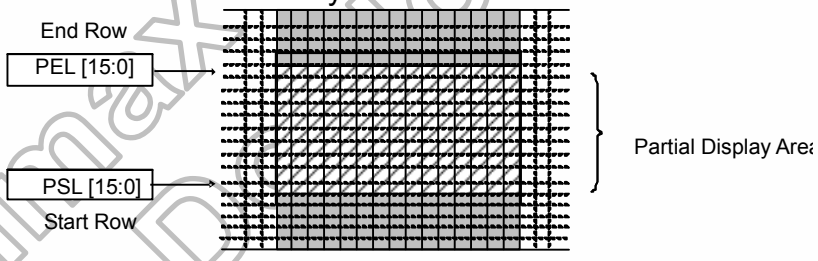
Figure 6. 15 Partial Area End Row Register Low Byte (R0Dh)

These commands (R0Ah~~0Dh) define the partial mode's display area. There are 4 parameters associated with this command, PSL[15:0], PEL[15:0], as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

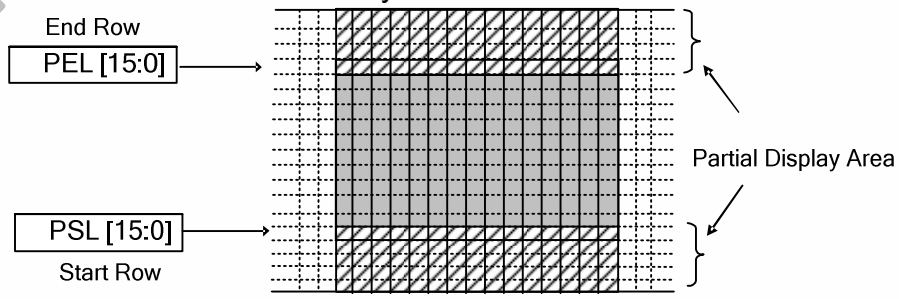
If End Row>Start Row when Memory Access Control GS=0



If End Row>Start Row when Memory Access Control GS=1



If End Row<Start Row when Memory Access Control GS=0



If End Row = Start Row then the Partial Area will be one row deep.

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6.11 Vertical scroll top fixed area register (R0E~0Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 6. 16 Vertical Scroll Top Fixed Area Register Upper Byte (R0Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 6. 17 Vertical Scroll Top Fixed Area Register Low Byte (R0Fh)

6.12 Vertical scroll height area register (R10~11h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 6. 18 Vertical Scroll Height Area Register Upper Byte (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 6. 19 Vertical Scroll Height Area Register Low Byte (R11h)

6.13 Vertical scroll button fixed area register (R12~13h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 6. 20 Vertical Scroll Button Fixed Area Register Upper Byte (R12h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 6. 21 Vertical Scroll Button Fixed Area Register Low Byte (R13h)

These commands (R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display. When Memory Access Control GS=0,

TFA[15..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

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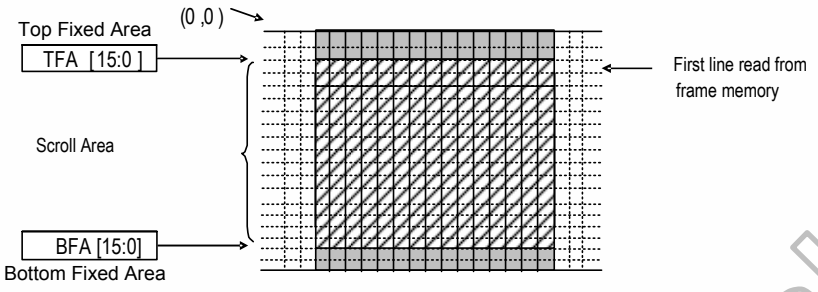
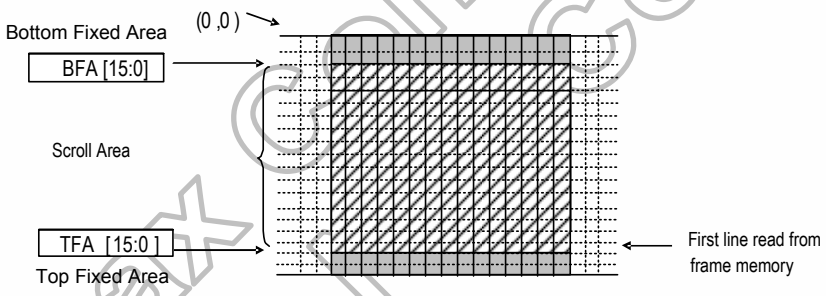
BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory Line Pointer.



When Memory Access Control GS=1,
TFA[15..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.
BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



6.14 Vertical scroll start address register (R14~15h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 6. 22 Vertical Scroll Start Address Register Upper Byte (R14h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

Figure 6. 23 Vertical Scroll Start Address Register Low Byte (R15h)

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes

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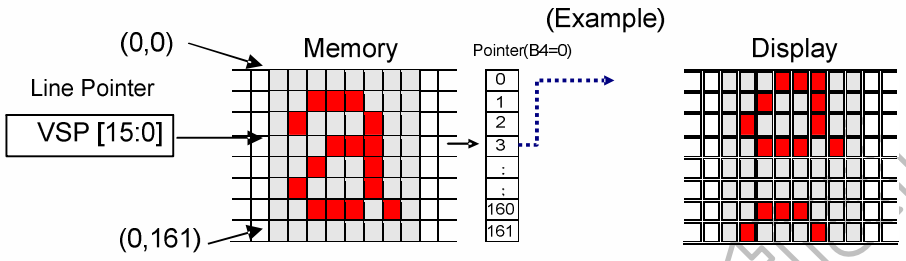
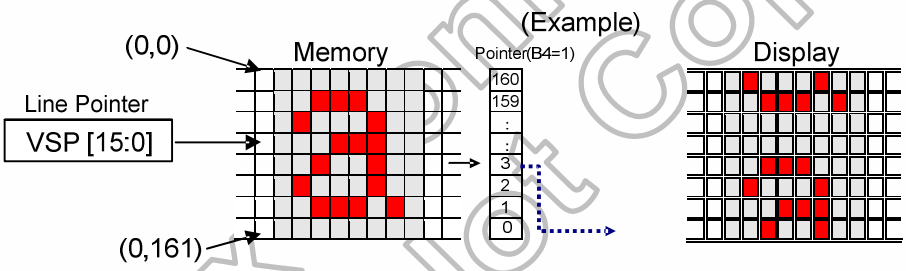
the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When Memory Access Control B4=0

Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP=3



When Memory Access Control B4=1

Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP=3



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
VSP refers to the Frame Memory line Pointer.

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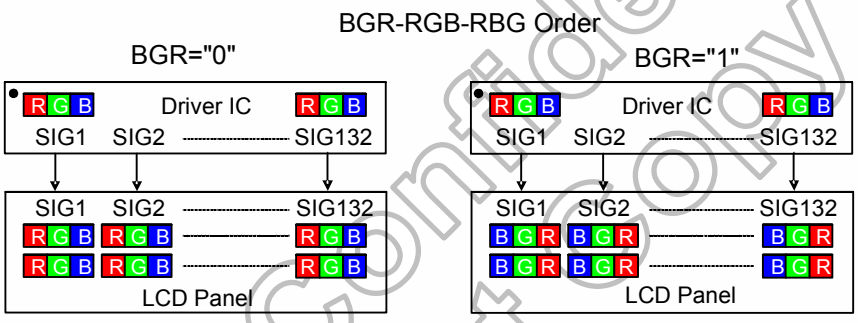
6.15 Memory access control register (R16h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	MY	MX	MV	GS	BGR	SS	SCROLL_EN	SM
R	1	*	*	*	*	*	*	*	*	MY	MX	MV	GS	BGR	SS	SCROLL_EN	SM

Figure 6. 24 Memory Access Control Register (R16h)

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. "MCU to memory write/read direction"
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)



GS: The gate driver output shift direction selected. When GS=0, the shift direction from G1 to G480. When GS = 1, the shift direction from G480 to G1.

SS: The source driver output shift direction selected. When SS=0, the shift direction from S1 to S720. When SS = 1, the shift direction from S720 to S1.

SCROLL_ON: Vertical Scrolling Function enable, High active.

SM: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin

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6.16 OSC control 1 register (R17h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	RADJ3	RADJ2	RADJ1	RADJ0	*	*	*	OSC_EN
R	1	*	*	*	*	*	*	*	*	RADJ3	RADJ2	RADJ1	RADJ0	*	*	*	OSC_EN

Figure 6. 25 OSC Control 1 Register (R17h)

This command is used to set internal oscillator related setting

RADJ[3:0]: Internal oscillator frequency adjust, default is 7.5MHz.

RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency
0	0	0	0	145%
0	0	0	1	140%
0	0	1	0	135%
0	0	1	1	130%
0	1	0	0	125%
0	1	0	1	120%
0	1	1	0	115%
0	1	1	1	110%
1	0	0	0	105%
1	0	0	1	100%
1	0	1	0	95%
1	0	1	1	90%
1	1	0	0	85%
1	1	0	1	80%
1	1	1	0	75%
1	1	1	1	70%

OSC_EN: Enable internal oscillator, High active.

6.17 OSC control 2 register (R18h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	UADJ2	UADJ1	UADJ0	CADJ3	CADJ2	CADJ1	CADJ0
R	1	*	*	*	*	*	*	*	*	*	UADJ2	UADJ1	UADJ0	CADJ3	CADJ2	CADJ1	CADJ0

Figure 6. 26 OSC Control 2 Register (R18h)

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6.18 Power control 1 register (R19h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GAS ENB	*	*	PON	DK	XDK	VLCD _TRI	STB
R	1	*	*	*	*	*	*	*	*	GAS ENB	*	*	PON	DK	XDK	VLCD _TRI	STB

Figure 6. 27 Power Control 1 Register (R19h)

GASENB: This stands for abnormal power-off supervisal function when the power is off. It's for monitoring power status by NISD pad when GASENB is set to 0.

PON: Specify on/off control of step-up circuit 2 for VGL voltage generation. For detail, see the Power Supply Setting Sequence.

PON	Operation of Step-up Circuit 2
0	OFF
1	ON

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DK: Specify on/off control of step-up circuit 1 for VLCD voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of Step-up Circuit 1
0	ON
1	OFF

STB: When STB = "1", the HX8352-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0").

In the standby mode, the GRAM data and register content are retained.

XDK, VLCD_TRI: Specify the ratio of step-up circuit for VLCD voltage generation.

VLCD_TRI	XDK	Step up circuit 1	Capacitor Connection Pins
0	0	2 x VCI	C11A, C11B
0	1	2 x VCI	C11A, C11B, CX11A, CX11B
1	0	3 x VCI	C11A, C11B, CX11A, CX11B
1	1	Setting inhabited	Setting inhabited

6.19 Power control 2 register (R1Ah)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	VC32	VC31	VC30	*	VC12	VC11	VC10
R	1	*	*	*	*	*	*	*	*	*	VC32	VC31	VC30	*	VC12	VC11	VC10

Figure 6. 28 Power Control 2 Register (R1Ah)

VC1(2-0): Specify the ratio of VBGP for VLCD voltage adjusting.

VC12	VC11	VC10	DDVDH
0	0	0	VBGP * 5.47
0	0	1	VBGP * 5.13
0	1	0	VBGP * 4.82
0	1	1	VBGP * 4.56
1	0	0	VBGP * 4.32
1	0	1	VBGP * 4.10
1	1	0	VBGP * 3.91
1	1	1	VBGP * 3.73

Note: (1) VBGP is the internal reference voltage equals to 1.25V
(2) When VLCD_TRI=1, DDVDH ≦ (3xVCI - 0.5V)
(3) When VLCD_TRI=0, DDVDH ≦ (2xVCI - 0.5V)

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VC3(2-0): Specify the reference voltage VREG3 (the factor of VCI) for VGL voltage adjusting

VC32	VC31	VC30	VREG3
0	0	0	VLCD
0	0	1	VBGPx4.494
0	1	0	VBGPx4.301
0	1	1	VBGPx4.124
1	0	0	VBGPx3.96
1	0	1	VBGPx3.774
1	1	0	VBGPx3.571
1	1	1	Hi-Z

Note: VREG3 < VLCD -0.5V

6.20 Power control 3 register (R1Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BT3	BT2	BT1	BT0	*	*	AP1	AP0
R	1	*	*	*	*	*	*	*	*	BT3	BT2	BT1	BT0	*	*	AP1	AP0

Figure 6. 29 Power Control 3 Register (R1Bh)

AP(2-0)

Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption, AP(2-0) can be set as “000” when display is off and the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP1	AP0	Constant Current of Operational
0	0	Power Circuit Off
0	1	0.67
1	0	0.67
1	1	0.67

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BT(3-0): Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT3	BT2	BT1	BT0	VCL	VGH	VGL		Capacitor Connection Pins
						VCOMG=1	VCOMG=0	
0	0	0	0	-1 x VCI	VREG3X3 [x 6]	-(VREG3X2)+VCL [x -5]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	0	0	1	-1 x VCI	VREG3X3 [x 6]	-(VREG3X2) [x -4]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	0	1	0	-1 x VCI	VREG3X3 [x 6]	-(VREG3+VCI) [x -3]	-(VREG3+VCI) [x -3]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	0	1	1	-1 x VCI	VREG3X2+VCI [x 5]	-(VREG3X2)+VCL [x -5]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	1	0	0	-1 x VCI	VREG3X2+VCI [x 5]	-(VREG3X2) [x -4]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	1	0	1	-1 x VCI	VREG3X2+VCI [x 5]	-(VREG3+VCI) [x -3]	-(VREG3+VCI) [x -3]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	1	1	0	-1 x VCI	VREG3X2 [x 4]	-(VREG3X2) [x -4]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
Other setting				Inhibited				

Note: (1) The conditions of VLCD ≦ 6V, VCL ≦ -3.3V, VGH-VGL ≦ 32V must be satisfied.
(2) If VCOMG=0, VCL output is float.

6.21 Power control 4 register (R1Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	PON	VRH 3	VRH 2	VRH 1	VRH 0
R	1	*	*	*	*	*	*	*	*	*	*	*	PON	VRH 3	VRH 2	VRH 1	VRH 0

Figure 6. 30 Power Control 4 Register (R1Ch)

VRH[3:0]: Set the magnification of amplification for VREG1 voltage for gamma voltage setting. It allows magnify the amplification of VBGP from 2.8 to 4.8 times.

VRH3	VRH2	VRH1	VRH0	VREG1
0	0	0	0	VBGPx 2.8
0	0	0	1	VBGP x 3.0
0	0	1	0	VBGP x 3.2
0	0	1	1	VBGP x 3.3
0	1	0	0	VBGP x 3.4
0	1	0	1	VBGP x 3.5
• •	• •	• •	• •	• •
1	0	0	1	VBGP x 3.9
1	0	1	0	VBGPx 4.0
1	0	1	1	VBGPx 4.2
1	1	0	0	VBGPx 4.4
1	1	0	1	VBGPx 4.6
1	1	1	0	VBGPx 4.8
1	1	1	1	Inhibited

Note: (1) VBGP is the internal reference voltage equals to 1.25V
(2) VREG1 ≦ (DDVDH – 0.5V).

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6.22 Power control 5 register (R1Dh)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	BGP3	BGP2	BGP1	BGP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	BGP3	BGP2	BGP1	BGP0

Figure 6. 31 Power Control 5 Register (R1Dh)

BGP[3:0]: band gap voltage control

BGP[3:0]	VBGP Output
4'b0000	X 0.936
4'b0001	X 0.944
4'b0010	X 0.952
4'b0011	X 0.96
4'b0100	X 0.968
4'b0101	X 0.976
4'b0110	X 0.984
4'b0111	X 0.992
4'b1000	**X 1.000**
4'b1001	X 1.008
4'b1010	X 1.016
4'b1011	X 1.024
4'b1100	X 1.032
4'b1101	X 1.040
4'b1110	X 1.048
4'b1111	X 1.056

6.23 Power control 6 register (R1Eh)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	*	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0
R	1	*	*	*	*	*	*	*	*	*	*	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0

Figure 6. 32 Power Control 6 Register (R1Eh)

VCOMG:
When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ VCL+0.3V). When VCOMG = 0, VCOML outputs VSSA and VDV(4-0) setting are invalid. Then, low power consumption is accomplished.

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VDV(4-0):

Specify the VCOM amplitude factors for panel common driving (VCOML= VCOMH – VCOM amplitude, VCOML ≥ VCL+0.3V). It is possible to setup from 0.6 to 1.23 times of VREG1. When VCOMG=0, the VDV(4-0) setup is invalid and VCOML is output VSSA

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	VREG1*0.6
0	0	0	0	1	VREG1*0.63
0	0	0	1	0	VREG1*0.66
0	0	0	1	1	VREG1*0.69
0	0	1	0	0	VREG1*0.72
0	0	1	0	1	VREG1*0.75
0	0	1	1	0	VREG1*0.78
0	0	1	1	1	VREG1*0.81
0	1	0	0	0	VREG1*0.84
0	1	0	0	1	VREG1*0.87
0	1	0	1	0	VREG1*0.9
0	1	0	1	1	VREG1*0.93
0	1	1	0	0	VREG1*0.96
0	1	1	0	1	VREG1*0.99
0	1	1	1	0	VREG1*1.02
0	1	1	1	1	Inhibit
1	0	0	0	0	VREG1*1.05
1	0	0	0	1	VREG1*1.08
1	0	0	1	0	VREG1*1.11
1	0	0	1	1	VREG1*1.14
1	0	1	0	0	VREG1*1.17
1	0	1	0	1	VREG1*1.2
1	0	1	1	0	VREG1*1.23
1	0	1	1	1	Inhibit
1	1	0	0	0	Inhibit
1	1	0	0	1	Inhibit
1	1	0	1	0	Inhibit
1	1	0	1	1	Inhibit
1	1	1	0	0	Inhibit
1	1	1	0	1	Inhibit
1	1	1	1	0	Inhibit
1	1	1	1	1	Inhibit

Note: VCOML ≧ (VCL + 0.3), VCOMH≦(DDVDH - 0.3) when set VDV[4:0]

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6.24 VCOM control register (R1Fh)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R	1	*	*	*	*	*	*	*	*	*	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 6. 33 VCOM Control Register (R1Fh)

VCM(6-0):

Set the VCOMH voltage (High level voltage of VCOM) It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VREG1 * 0.4
0	0	0	0	0	0	1	VREG1 * 0.405
0	0	0	0	0	1	0	VREG1 * 0.41
0	0	0	0	0	1	1	VREG1 * 0.415
0	0	0	0	1	0	0	VREG1 * 0.42
0	0	0	0	1	0	1	VREG1 * 0.425
0	0	0	0	1	1	0	VREG1 * 0.43
0	0	0	0	1	1	1	VREG1 * 0.435
0	0	0	1	0	0	0	VREG1 * 0.44
0	0	0	1	0	0	1	VREG1 * 0.445
0	0	0	1	0	1	0	VREG1 * 0.45
0	0	0	1	0	1	1	VREG1 * 0.455
0	0	0	1	1	0	0	VREG1 * 0.46
0	0	0	1	1	0	1	VREG1 * 0.465
0	0	0	1	1	1	0	VREG1 * 0.47
0	0	0	1	1	1	1	VREG1 * 0.475
0	0	1	0	0	0	0	VREG1 * 0.48
0	0	1	0	0	0	1	VREG1 * 0.485
0	0	1	0	0	1	0	VREG1 * 0.49
0	0	1	0	0	1	1	VREG1 * 0.495
0	0	1	0	1	0	0	VREG1 * 0.5
0	0	1	0	1	0	1	VREG1 * 0.505
0	0	1	0	1	1	0	VREG1 * 0.51
0	0	1	0	1	1	1	VREG1 * 0.515
0	0	1	1	0	0	0	VREG1 * 0.52
0	0	1	1	0	0	1	VREG1 * 0.525
0	0	1	1	0	1	0	VREG1 * 0.53
0	0	1	1	0	1	1	VREG1 * 0.535
0	0	1	1	1	0	0	VREG1 * 0.54
0	0	1	1	1	0	1	VREG1 * 0.545
0	0	1	1	1	1	0	VREG1 * 0.55
0	0	1	1	1	1	1	VREG1 * 0.555
0	1	0	0	0	0	0	VREG1 * 0.56
0	1	0	0	0	0	1	VREG1 * 0.565
0	1	0	0	0	1	0	VREG1 * 0.57
0	1	0	0	0	1	1	VREG1 * 0.575
0	1	0	0	1	0	0	VREG1 * 0.58
0	1	0	0	1	0	1	VREG1 * 0.585
0	1	0	0	1	1	0	VREG1 * 0.59
0	1	0	0	1	1	1	VREG1 * 0.595
0	1	0	1	0	0	0	VREG1 * 0.6
0	1	0	1	0	0	1	VREG1 * 0.605
0	1	0	1	0	1	0	VREG1 * 0.61
0	1	0	1	0	1	1	VREG1 * 0.615
0	1	0	1	1	0	0	VREG1 * 0.62
0	1	0	1	1	0	1	VREG1 * 0.625
0	1	0	1	1	1	0	VREG1 * 0.63
0	1	0	1	1	1	1	VREG1 * 0.635
0	1	1	0	0	0	0	VREG1 * 0.64
0	1	1	0	0	0	1	VREG1 * 0.645
0	1	1	0	0	1	0	VREG1 * 0.65
0	1	1	0	0	1	1	VREG1 * 0.655
0	1	1	0	1	0	0	VREG1 * 0.66
0	1	1	0	1	0	1	VREG1 * 0.665
0	1	1	0	1	1	0	VREG1 * 0.67
0	1	1	0	1	1	1	VREG1 * 0.675

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VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	1	1	1	0	0	0	VREG1 * 0.68
0	1	1	1	0	0	1	VREG1 * 0.685
0	1	1	1	0	1	0	VREG1 * 0.69
0	1	1	1	0	1	1	VREG1 * 0.695
0	1	1	1	1	0	0	VREG1 * 0.7
0	1	1	1	1	0	1	VREG1 * 0.705
0	1	1	1	1	1	0	VREG1 * 0.71
0	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister),
1	0	0	0	0	0	0	VREG1 * 0.715
1	0	0	0	0	0	1	VREG1 * 0.72
1	0	0	0	0	1	0	VREG1 * 0.725
1	0	0	0	0	1	1	VREG1 * 0.73
1	0	0	0	1	0	0	VREG1 * 0.735
1	0	0	0	1	0	1	VREG1 * 0.74
1	0	0	0	1	1	0	VREG1 * 0.745
1	0	0	0	1	1	1	VREG1 * 0.75
1	0	0	1	0	0	0	VREG1 * 0.755
1	0	0	1	0	0	1	VREG1 * 0.76
1	0	0	1	0	1	0	VREG1 * 0.765
1	0	0	1	0	1	1	VREG1 * 0.77
1	0	0	1	1	0	0	VREG1 * 0.775
1	0	0	1	1	0	1	VREG1 * 0.78
1	0	0	1	1	1	0	VREG1 * 0.785
1	0	0	1	1	1	1	VREG1 * 0.79
1	0	1	0	0	0	0	VREG1 * 0.795
1	0	1	0	0	0	1	VREG1 * 0.8
1	0	1	0	0	1	0	VREG1 * 0.805
1	0	1	0	0	1	1	VREG1 * 0.81
1	0	1	0	1	0	0	VREG1 * 0.815
1	0	1	0	1	0	1	VREG1 * 0.82
1	0	1	0	1	1	0	VREG1 * 0.825
1	0	1	0	1	1	1	VREG1 * 0.83
1	0	1	1	0	0	0	VREG1 * 0.835
1	0	1	1	0	0	1	VREG1 * 0.84
1	0	1	1	0	1	0	VREG1 * 0.845
1	0	1	1	0	1	1	VREG1 * 0.85
1	0	1	1	1	0	0	VREG1 * 0.855
1	0	1	1	1	0	1	VREG1 * 0.86
1	0	1	1	1	1	0	VREG1 * 0.865
1	0	1	1	1	1	1	VREG1 * 0.87
1	1	0	0	0	0	0	VREG1 * 0.875
1	1	0	0	0	0	1	VREG1 * 0.88
1	1	0	0	0	1	0	VREG1 * 0.885
1	1	0	0	0	1	1	VREG1 * 0.89
1	1	0	0	1	0	0	VREG1 * 0.895
1	1	0	0	1	0	1	VREG1 * 0.9
1	1	0	0	1	1	0	VREG1 * 0.905
1	1	0	0	1	1	1	VREG1 * 0.91
1	1	0	1	0	0	0	VREG1 * 0.915
1	1	0	1	0	0	1	VREG1 * 0.92
1	1	0	1	0	1	0	VREG1 * 0.925
1	1	0	1	0	1	1	VREG1 * 0.93
1	1	0	1	1	0	0	VREG1 * 0.935
1	1	0	1	1	0	1	VREG1 * 0.94
1	1	0	1	1	1	0	VREG1 * 0.945
1	1	0	1	1	1	1	VREG1 * 0.95
1	1	1	0	0	0	0	VREG1 * 0.955
1	1	1	0	0	0	1	VREG1 * 0.96
1	1	1	0	0	1	0	VREG1 * 0.965
1	1	1	0	0	1	1	VREG1 * 0.97
1	1	1	0	1	0	0	VREG1 * 0.975
1	1	1	0	1	0	1	VREG1 * 0.98

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VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
1	1	1	0	1	1	0	inhibit
1	1	1	0	1	1	1	inhibit
1	1	1	1	0	0	0	inhibit
1	1	1	1	0	0	1	inhibit
1	1	1	1	0	1	0	inhibit
1	1	1	1	0	1	1	inhibit
1	1	1	1	1	0	0	inhibit
1	1	1	1	1	0	1	inhibit
1	1	1	1	1	1	0	inhibit
1	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister)

6.25 Read data register (R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Figure 6. 34 Read Data Register (R22h)

RD17-0: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

Write data register (R22h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Figure 6. 35 Write Data Register (R22h)

WD[15:0]: Transforms the data into 16-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the MV, MX and MY bits.

Note: When IC received R22h, then HX8352-A didn't re-set to start address. If start address want re-set again, then SC (R02h~R03h) and SP (R06h~R07h) register need to re-set again.

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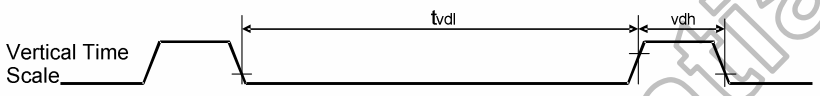
6.26 Display control 1 register (R23h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TEMODE	TEON
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TEMODE	TEON

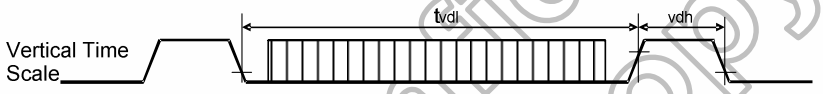
Figure 6. 36 Display Control Register (R23h)

TEMODE: Specify the Tearing-Effect mode.

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only.



When TEMODE =1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information



Note: During Sleep in Mode with Tearing Effect Line On, Tearing Effect Output pin active low

TEON:
This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing Memory Access Control bit B4.

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6.27 Display control 2 register (R24h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*
R	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*

Figure 6. 37 Display Control 2 Register (R24h)

PT[1:0]: Non-display area source output control see follow table

INVON /REV_PANEL	GRAM Data	Source Output Level							
		Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	18'h00000 : 18'h3FFFF	V63 : V0	V0 : V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z
1	18'h00000 : 18'h3FFFF	V0 : V63	V63 : V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z

D[1:0]: When D1=1, display is on; when D1=0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8352-A can control the charging current for the LCD with AC driving. When D1–0 = 01, the internal display of the HX8352-A is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

GON, DTE: Gate output select.

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

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6.28 Display control 3~8 register (R25h~R2Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_FP 7	N_FP 6	N_FP 5	N_FP 4	N_FP 3	N_FP 2	N_FP 1	N_FP 0
R	1	*	*	*	*	*	*	*	*	N_FP 7	N_FP 6	N_FP 5	N_FP 4	N_FP 3	N_FP 2	N_FP 1	N_FP 0

Figure 6. 38 Display Control 2 Register (R25h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_FP 7	P_FP 6	P_FP 5	P_FP 4	P_FP 3	P_FP 2	P_FP 1	P_FP 0
R	1	*	*	*	*	*	*	*	*	P_FP 7	P_FP 6	P_FP 5	P_FP 4	P_FP 3	P_FP 2	P_FP 1	P_FP 0

Figure 6. 39 Display Control 3 Register (R26h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_FP 7	I_FP 6	I_FP 5	I_FP 4	I_FP 3	I_FP 2	I_FP 1	I_FP 0
R	1	*	*	*	*	*	*	*	*	I_FP 7	I_FP 6	I_FP 5	I_FP 4	I_FP 3	I_FP 2	I_FP 1	I_FP 0

Figure 6. 40 Display Control 4 Register (R27h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_BP 7	N_BP 6	N_BP 5	N_BP 4	N_BP 3	N_BP 2	N_BP 1	N_BP 0
R	1	*	*	*	*	*	*	*	*	N_BP 7	N_BP 6	N_BP 5	N_BP 4	N_BP 3	N_BP 2	N_BP 1	N_BP 0

Figure 6. 41 Display Control 5 Register (R28h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_BP 7	I_BP 6	I_BP 5	I_BP 4	I_BP 3	I_BP 2	I_BP 1	I_BP 0
R	1	*	*	*	*	*	*	*	*	I_BP 7	I_BP 6	I_BP 5	I_BP 4	I_BP 3	I_BP 2	I_BP 1	I_BP 0

Figure 6. 42 Display Control 6 Register (R29h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_BP 7	I_BP 6	I_BP 5	I_BP 4	I_BP 3	I_BP 2	I_BP 1	I_BP 0
R	1	*	*	*	*	*	*	*	*	I_BP 7	I_BP 6	I_BP 5	I_BP 4	I_BP 3	I_BP 2	I_BP 1	I_BP 0

Figure 6. 43 Display Control 7 Register (R2Ah)

N_BP, N_FP: Back Porch and Front Porch setting in Normal mode
P_BP, P_FP: Back Porch and Front Porch setting in Partial mode
I_BP, I_FP: Back Porch and Front Porch setting in Idle mode

FP[7:0]: Specify the amount of scan line for front porch (FP).
BP[7:0]: Specify the amount of scan line for back porch (BP).

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FP[7:0] BP[7:0]	Number of FP +BP Line
00000000	Ignore
00000001	Ignore
00000010	3 Lines
00000011	5 Lines
00000100	6 Lines
00000101	9 Lines
00000110	11 Lines
: : :	: : :
11111010	499 Lines
11111011	501 Lines
11111100	503 Lines
11111101	505 Lines
11111110	507Lines
11111111	509 Lines

Note: BP[7:0] ≤ FP[7:0]

Operation Mode	BP	FP	BP + FP
System Interface	≥2 lines	≥2 lines	≤ 16 lines

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6.29 Cycle control 1~3 register (R2B~2Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_DC 7	N_DC 6	N_DC 5	N_DC 4	N_DC 3	N_DC 2	N_DC 1	N_DC 0
R	1	*	*	*	*	*	*	*	*	N_DC 7	N_DC 6	N_DC 5	N_DC 4	N_DC 3	N_DC 2	N_DC 1	N_DC 0

Figure 6. 44 Cycle Control 1 Register (R2Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_DC 7	P_DC 6	P_DC 5	P_DC 4	P_DC 3	P_DC2	P_DC 1	P_DC 0
R	1	*	*	*	*	*	*	*	*	P_DC 7	P_DC 6	P_DC 5	P_DC 4	P_DC 3	P_DC2	P_DC 1	P_DC 0

Figure 6. 45 Cycle Control 2 Register (R2Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_DC 7	I_DC 6	I_DC 5	I_DC 4	I_DC 3	I_DC 2	I_DC 1	I_DC 0
R	1	*	*	*	*	*	*	*	*	I_DC 7	I_DC 6	I_DC 5	I_DC 4	I_DC 3	I_DC 2	I_DC 1	I_DC 0

Figure 6. 46 Cycle Control 3 Register (R2Dh)

N_DC: Normal mode
P_DC: Partial mode
I_DC: Idle mode

DC(7-0): specify the clock frequency for DC/DC converter operating.

fosc= R-C oscillation frequency

DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCDCf
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	fosc
0	0	0	0	0	0	1	0	fosc/ 2
:								:
1	1	1	1	1	1	1	0	fosc/ 254
1	1	1	1	1	1	1	1	fosc / 255

Note: It is recommended to set DC(7-0) as "20"h, which means one charge bump clock periodis 32 internal oscillation clocks.

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6.30 Cycle control 4~8 register (R2E~32h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	FS11	FS10	FS01	FS00	I_TRN3	I_RTN2	I_RTN1	I_RTN0
R	1	*	*	*	*	*	*	*	*	FS11	FS10	FS01	FS00	I_RTN3	I_RTN2	I_RTN1	I_RTN0

Figure 6. 47 Cycle Control 4 Register (R2Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_RTN3	P_RTN2	P_RTN1	P_RTN0	N_RTN3	N_RTN2	N_RTN1	N_RTN0
R	1	*	*	*	*	*	*	*	*	P_RTN3	P_RTN2	P_RTN1	P_RTN0	N_RTN3	N_RTN2	N_RTN1	N_RTN0

Figure 6. 48 Cycle Control 5 Register (R2Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	DIV_I1	DIV_I0	*	*	*	I_NW
R	1	*	*	*	*	*	*	*	*	*	*	DIV_I1	DIV_I0	*	*	*	I_NW

Figure 6. 49 Cycle Control 1 Register (R30h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	DIV_N1	DIV_N0	*	*	*	N_NW
R	1	*	*	*	*	*	*	*	*	*	*	DIV_N1	DIV_N0	*	*	*	N_NW

Figure 6. 50 Cycle Control 2 Register (R31h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	DIV_P1	DIV_P0	*	*	*	P_NW
R	1	*	*	*	*	*	*	*	*	*	*	DIV_P1	DIV_P0	*	*	*	P_NW

Figure 6. 51 Cycle Control 3 Register (R32h)

FS0(1-0): Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for VLCD voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

FS01	FS0	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

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FS1(1-0): Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL, VCL voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

N_ NW, N_ RTN: Normal mode
P_ NW , P_ RTN: Partial mode
I_ NW, I_ RTN: Idle mode

The driver IC support individual inversion type and clock per line for Normal display mode, Partial display mode and Idle (8-color) display mode. The resultant NW and RTN will be selected automatically according display mode.

NW: Frame Inversion and Line inversion control for display.

NW	Inversion Type
0	Frame inversion
1	Lline inversion

RTN[3:0]: Set the 1-line period in a clock unit for normal display mode.

Clock cycles=1/internal operation clock frequency

RTN[3:0]	Clock Cycles per Line
4'b0000	249
4'b0001	250
4'b0010	251
4'b0011	252
….	….
4'b1110	263
4'b1111	264

DIV_N1-0: The division ratio of clocks for Normal mode internal operation (DIV1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV_N1-0. Frame frequency can be adjusted along with the 1H period (N_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

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DIV_P1-0: The division ratio of clocks for Partial mode internal operation (DIV_P1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV_P1-0. Frame frequency can be adjusted along with the 1H period (P_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

DIV_I1-0: The division ratio of clocks for Idle mode internal operation (DIV_I1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV_I1-0. Frame frequency can be adjusted along with the 1H period (I_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV_N1 / DIV_P1 / DIV_I1	DIV_N0 / DIV_P0 / DIV_I0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Formula for the Frame Frequency:

Frame frequency = fosc/ (RTN × DIV × (NL+BP+FP)) [HZ]

fosc: RC oscillation frequency

6.31 Cycle control 10 register (R34h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EQS 7	EQS 6	EQS 5	EQS 4	EQS 3	EQS 2	EQS 1	EQS 0
R	1	*	*	*	*	*	*	*	*	EQS 7	EQS 6	EQS 5	EQS 4	EQS 3	EQS 2	EQS 1	EQS 0

Figure 6. 52 Cycle Control 10 Register (R34h)

EQS[7:0] : Internal used and Not open.

6.32 Cycle control 11 register (R35h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EQP 7	EQP 6	EQP 5	EQP 4	EQP 3	EQP 2	EQP 1	EQP 0
R	1	*	*	*	*	*	*	*	*	EQP 7	EQP 6	EQP 5	EQP 4	EQP 3	EQP 2	EQP 1	EQP 0

Figure 6. 53 Cycle Control 11 Register (R35h)

EQP[7:0] : Internal used and Not open.

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6.33 Cycle control 12 register (R36h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
R	1	*	*	*	*	*	*	*	*	*	*	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

Figure 6. 54 Cycle Control 12 Register (R36h)

PTG[1:0]: Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

ISC[3:0]: Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 70Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

6.34 Cycle control 13~15 register (R37h~39h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0
R	1	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0

Figure 6. 55 Display Control 5 Register (R37h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GDON 7	GDON 6	GDON 5	GDON 4	GDON 3	GDON 2	GDON 1	GDON 0
R	1	*	*	*	*	*	*	*	*	GDON 7	GDON 6	GDON 5	GDON 4	GDON 3	GDON 2	GDON 1	GDON 0

Figure 6. 56 Display Control 6 Register (R38h)

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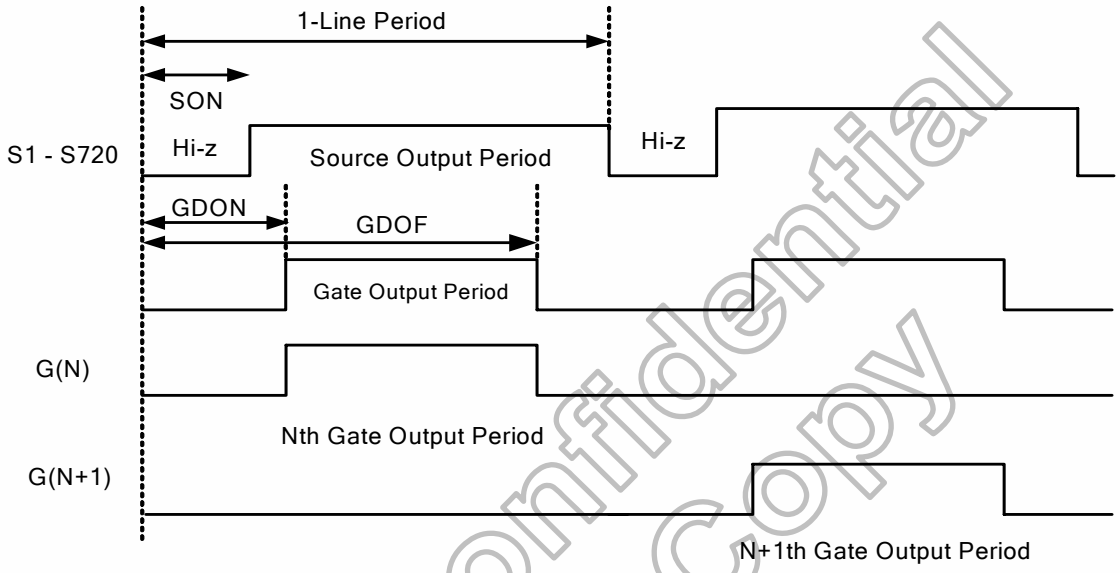
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GDOF 7	GDOF 6	GDOF 5	GDOF 4	GDOF 3	GDOF 2	GDOF 1	GDOF 0
R	1	*	*	*	*	*	*	*	*	GDOF 7	GDOF 6	GDOF 5	GDOF 4	GDOF 3	GDOF 2	GDOF 1	GDOF 0

Figure 6. 57 Display Control 3 Register (R39h)

The HX8352-A can control the display operation period time for LCD panel driving as follow:



SON7-0: Specify the valid source output start time in 1-line driving period. The period time is defined as SYSCLK clock number. (Please note that the setting “00h” and “01h” is inhibited)**.**

GDON7-0: Specify the valid gate output start time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited)**.**

GDOF7-0: Specify the gate output end time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the GDOF7-0 ≤ HCK-1).

6.35 Interface control 1 register (R3Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CSEL 2	CSEL 1	CSEL 0	*	DPL	HSPL	VSPL	EPL
R	1	*	*	*	*	*	*	*	*	CSEL 2	CSEL 1	CSEL 0	*	DPL	HSPL	VSPL	EPL

Figure 6. 58 Interface Control 1 Register (R3Ah)

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This command is used to set RGB interface and Serial bus interface related register

CSEL: RGB interface data format select.

Interface Format	CSEL2	CSEL1	CSEL0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

EPL: Specify the polarity of Enable pin in RGB interface mode. EPL=0, the Enable is High active; EPL=1, the Enable is Low active

VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

DPL: The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

6.36 Source control 1~2 register (R3Ch~3Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_SAP[7:0]							
R	1	*	*	*	*	*	*	*	*	N_SAP[7:0]							

Figure 6. 59 Source Control 1 Register (R3Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_SAP[7:0]							
R	1	*	*	*	*	*	*	*	*	I_SAP[7:0]							

Figure 6. 60 Source Control 2 Register (R3Dh)

N_SAP[7:0]: Normal mode
I_SAP[7:0]: Idle mode
SAP[7:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the source driver. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. The tradeoff is between display quality and current consumption. During no display operation, when SAP[7–0] = 0x00h, the current consumption can be reduced by stopping the operational amplifier.

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N_SAP[7:0] / I_SAP[7:0]								Source driving ability Turn Off time
0	0	0	0	0	0	0	0	Source output all stop
0	0	0	0	0	0	0	1	1- clock
0	0	0	0	0	0	1	0	2- clock
0	0	0	0	0	0	1	1	3- clock
0	0	0	0	0	1	0	0	4- clock
0	0	0	0	0	1	0	1	5- clock
0	0	0	0	0	1	1	0	6- clock
0	0	0	0	0	1	1	1	7- clock
- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	
1	1	1	1	1	0	0	1	249- clock
1	1	1	1	1	0	1	0	250- clock
1	1	1	1	1	0	1	1	251- clock
1	1	1	1	1	1	0	0	252- clock
1	1	1	1	1	1	0	1	253- clock
1	1	1	1	1	1	1	0	254- clock
1	1	1	1	1	1	1	1	255- clock

6.37 GAMMA control 1~12 register (R3E~49h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GSEL	CP12	CP11	CP10	*	CP02	CP01	CP00
R	1	*	*	*	*	*	*	*	*	GSEL	CP12	CP11	CP10	*	CP02	CP01	CP00

Figure 6. 61 GAMMA Control 1 Register (R3Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	CN12	CN11	CN10	*	CN02	CN01	CN00
R	1	*	*	*	*	*	*	*	*	*	CN12	CN11	CN10	*	CN02	CN01	CN00

Figure 6. 62 GAMMA Control 2 Register (R3Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NP12	NP11	NP10	*	NP02	NP01	NP00
R	1	*	*	*	*	*	*	*	*	*	NP12	NP11	NP10	*	NP02	NP01	NP00

Figure 6. 63 GAMMA Control 3 Register (R40h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NP32	NP31	NP30	*	NP22	NP21	NP20
R	1	*	*	*	*	*	*	*	*	*	NP32	NP31	NP30	*	NP22	NP21	NP20

Figure 6. 64 GAMMA Control 4 Register (R41h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NP52	NP51	NP50	*	NP42	NP41	NP40
R	1	*	*	*	*	*	*	*	*	*	NP52	NP51	NP50	*	NP42	NP41	NP40

Figure 6. 65 GAMMA Control 5 Register (R42h)

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R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NN12	NN11	NN10	*	NN02	NN01	NN00
R	1	*	*	*	*	*	*	*	*	*	NN12	NN11	NN10	*	NN02	NN01	NN00

Figure 6. 66 GAMMA Control 6 Register (R43h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NN32	NN31	NN30	*	NN22	NN21	NN20
R	1	*	*	*	*	*	*	*	*	*	NN32	NN31	NN30	*	NN22	NN21	NN20

Figure 6. 67 GAMMA Control 7 Register (R44h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NN52	NN51	NN50	*	NN52	NN51	NN50
R	1	*	*	*	*	*	*	*	*	*	NN52	NN51	NN50	*	NN52	NN51	NN50

Figure 6. 68 GAMMA Control8 Register (R45h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGMP11	CGMP10	CGMP01	CGMP00	OP03	OP02	OP01	OP00
R	1	*	*	*	*	*	*	*	*	CGMP11	CGMP10	CGMP01	CGMP00	OP03	OP02	OP01	OP00

Figure 6. 69 GAMMA Control 9 Register (R46h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGMP3	CGMP2	*	OP14	OP13	OP12	OP11	OP10
R	1	*	*	*	*	*	*	*	*	CGMP3	CGMP2	*	OP14	OP13	OP12	OP11	OP10

Figure 6. 70 GAMMA Control 10 Register (R47h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGMN10	CGMN10	CGMN01	CGMN00	ON03	ON02	ON01	ON00
R	1	*	*	*	*	*	*	*	*	CGMN10	CGMN10	CGMN01	CGMN00	ON03	ON02	ON01	ON00

Figure 6. 71 GAMMA Control 11 Register (R48h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGMN3	CGMN2	*	ON14	ON13	ON12	ON11	ON10
R	1	*	*	*	*	*	*	*	*	CGMN3	CGMN2	*	ON14	ON13	ON12	ON11	ON10

Figure 6. 72 GAMMA Control 12 Register (R49h)

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CP1-0 [2:0]: Gamma Center Adjustment registers for positive polarity output
CN1-0 [2:0]: Gamma Center Adjustment registers for negative polarity output
NP5-0 [2:0]: Gamma Macro Adjustment registers for positive polarity output
NN5-0 [2:0]: Gamma Macro Adjustment registers for negative polarity output
OP0 [3:0]/OP1 [4:0]: Gamma Offset Adjustment register for positive polarity output
ON0 [3:0]/ON1 [4:0]: Gamma Offset Adjustment register for negative polarity output
CGMP0[1:0], CGMP1[1:0]: Gamma Tap Adjustment register for positive polarity output
CGMN0[1:0], CGMN1[1:0]: Gamma Tap Adjustment register for negative polarity output
CGMP2, CGMP3: Gamma Harmony adjustment registers for positive polarity output
CGMN2, CGMN3: Gamma Harmony adjustment registers for negative polarity output
GSEL: V0, V256 reference voltage selection. GSEL=1, V0=VgP/N0, V63= VgP/N7; If GSEL=0, V0=VREG1, V63= VGS. For details, please refer to 5.9.4 Gamma resister stream and 8 to 1 Selector.

This command is used to set Gamma Curve Related Setting

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	NP0 2-0	NN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	NP1 2-0	NN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	NP2 2-0	NN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	NP3 2-0	NN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	NP4 2-0	NN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	NP5 2-0	NN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

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6.38 Panel control register (R55h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
R	1	*	*	*	*	*	*	*	*	*	*	*	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL

Figure 6. 73 Panel Control Register (R55h)

BGR_PANEL: RGB-BGR ORDER set of Panel, Please refer BGR bit.
REV_PANEL: Display inversion mode of Panel, Please refer INVON bit.
SS_PANEL: The source driver output shift direction selected of Panel, Please refer SS bit.
SM_PANEL: Gate driver scan order of Panel, Please refer SM bit.
GS_PANEL: Vertical ORDER set of Panel, Please refer GS bit.

6.39 OTP related register 1 (R56h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_INDEX7	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0
R	1	*	*	*	*	*	*	*	*	OTP_INDEX7	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0

Figure 6. 74 OTP Related Register 1 (R56h)

OTP_INDEX[7:0]: Set location of OTP programming.

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6.40 OTP related register 2 (R57h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_MASK 7	OTP_MASK 6	OTP_MASK 5	OTP_MASK 4	OTP_MASK 3	OTP_MASK 2	OTP_MASK 1	OTP_MASK 0
R	1	*	*	*	*	*	*	*	*	OTP_MASK 7	OTP_MASK 6	OTP_MASK 5	OTP_MASK 4	OTP_MASK 3	OTP_MASK 2	OTP_MASK 1	OTP_MASK 0

Figure 6. 75 OTP Related Register 1 (R57h)

OTP_MASK7 [7:0]: Bit programming mask, if set to 1, it means that it doesn't program this bit

6.41 OTP related register 3 (R58h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	*	VPP_SEL	OTP_PROG
R	1	*	*	*	*	*	*	*	*	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	*	VPP_SEL	OTP_PROG

Figure 6. 76 OTP Related Register 3 (R58h)

OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the HW RESET is received. Nevertheless, if this bit was set to 1, it would disable the auto loading function when the HW RESET was received. In general, this bit is used when OTP is not yet programmed.

DCCLK_DISABLE: When written to 1, disable internal pumping Clock.

VPP_SEL: When it set to 1, VGH voltage is fed to OTP

OTP_PROG: When it set to 1, the internal registers begin to write to OTP.

6.42 OTP related register 4 (R59h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	*	*	*	*	*	*	*	*	OTP_DATA 7	OTP_DATA 6	OTP_DATA 5	OTP_DATA 4	OTP_DATA 3	OTP_DATA 2	OTP_DATA 1	OTP_DATA 0

Figure 6. 77 OTP Related Register 4 (R59h)

OTP_DATA: The OTP memory data and read only.

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6.43 IP control register (R5Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DGC_EN
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DGC_EN

Figure 6. 78 IP Control Register (R5Ah)

DGC_EN: Digital gamma correction enable.
0: Disable
1: Enable

6.44 DGC LUT register (R5Ch)

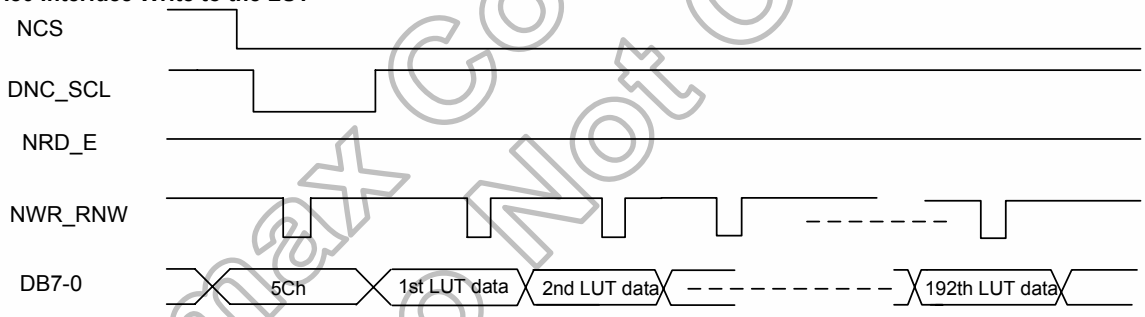
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	D7	D6	D5	D4	D3	D2	D1	D0

Figure 6. 79 DGC LUT WRITE Register (R5Ch)

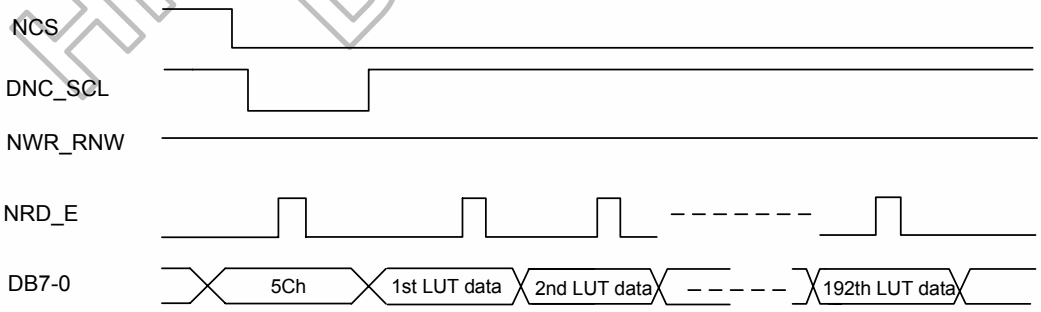
The command is to set digital gamma correction LUT, there are 192 words has to setting. The follow is timing of write LUT and LUT address range.

Note: This register just can support write function not support Read function.

I80 Interface Write to the LUT



M68 Interface Write to the LUT



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LUT	D7	D6	D5	D4	D3	D2	D1	D0
1st	R007	R006	R005	R004	R003	R002	R001	R000
2nd	R017	R016	R015	R014	R013	R012	R011	R010
:	:	:	:	:	:	:	:	:
63	R627	R626	R625	R624	R623	R622	R621	R620
64	R637	R636	R635	R634	R633	R632	R631	R630
65	G007	G006	G005	G004	G003	G002	G001	G000
66	G017	G016	G015	G014	G013	G012	G011	G010
:	:	:	:	:	:	:	:	:
127	G627	G626	G625	G624	G623	G622	G621	G620
128	G637	G636	G635	G634	G633	G632	G631	G630
129	B007	B006	B005	B004	B003	B002	B001	B000
130	B017	B016	B015	B014	B013	B012	B011	B010
:	:	:	:	:	:	:	:	:
101	B627	B626	B625	B624	B623	B622	B621	B620
192	B637	B636	B635	B634	B633	B632	B631	B630

6.45 Test mode control register (R83h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	0	TEST_MODE	0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	0	TEST_MODE	0

Figure 6. 80 TEST MODE Control Register (R83h)

When **TEST_MODE=1**, then in-housedregister can updated new setting.

6.46 VDDD control register (R85h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VDC_SEL2	VDC_SEL1	VDC_SEL0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VDC_SEL2	VDC_SEL1	VDC_SEL0

Figure 6. 81 VDDD Control Register (R85h)

VDC_SEL(2-0): VDDD will increase or reduce by VDC_SEL setting.

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6.47 Power driving control register (R8Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	0	0	0	0	PTBA2	PTBA1	PTBA0
R	1	*	*	*	*	*	*	*	*	0	0	0	0	0	PTBA2	PTBA1	PTBA0

Figure 6. 82 Power driving control register (R8Ah)

Resistor Setting	Power driving ability
PTBA[2:0]	AP[1:0]=01/10/11
000	0.00Iref
001	0.17Iref
010	0.33Iref
011	0.50Iref
100	0.67Iref
101	0.83Iref
110	1.00Iref
111	1.17Iref

6.48 Source gamma resistor setting register (R8B~R8Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	GS_Res1
R	1	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	GS_Res1

Figure 6. 83 Source Gamma resistor setting 1 Register (R8Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GS_Res0	0	0	1	0	0	1	1
R	1	*	*	*	*	*	*	*	*	GS_Res0	0	0	1	0	0	1	1

Figure 6. 84 Source Gamma resistor setting 2 Register (R8Ch)

Resistor Setting		Resistor
GS_RES0	GS_RES1	
0	X	0 ohm
1	0	120K ohm
1	1	60K ohm

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6.49 SYNC function register (R91h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	DCCLK_SYNC
R	1	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	DCCLK_SYNC

Figure 6. 85 SYNC Function Register (R91h)

DCDCLK_SYNC: Control synchronous function between DCDC_CLK and Display CLK.
DCDCLK_SYC=1, function Enable.
DCDCLK_SYC=0, function Disable.

6.50 PWM control 1 register (R95h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
R	1	*	*	*	*	*	*	*	*	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

Figure 6. 86 PWM Control 1 Register (R95h)

DBV[7:0]	Duty Cycle
0	1/255
1	2/255
2	3/255
3	4/255
:	:
:	:
252	252/255
253	253/255
254	254/255
255	255/255

Note: If BCTRL=0, then DBV[7:0]=0x00h.

6.50 PWM control 2 register (R96h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	BCTRL	0	0	BL	0	0
R	1	*	*	*	*	*	*	*	*	*	*	BCTRL	0	0	BL	0	0

Figure 6. 87 PWM Control 2 Register (R96h)

BL=1, Backlight control circuit turn on.
BCTRL=0, the DBV[7:0]=0x00h.
BCTRL=1, the DBV[7:0] can be active.

Note: The frequency of PWM is 300Hz.

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6.51 PWM control 3 register (R97h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	C1	C0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	C1	C0

Figure 6. 88 PWM Control 2 Register (R96h)

C[1:0]	CABC Mode	Note
00	CABC Off/ Mannual Mode	-
01	UI Mode	The display pattern is belong pattern of Text
10	Still Mode	The display is belong pattern of true color
11	Moving Mode	The patter nis belong pattern of Moving

6.52 CABC PWM period control 1 Register (R6Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	1	1	1	0	1	SEL_ PWM CLK2	SEL_ PWM CLK1	SEL_ PWM CLK0
R	1	*	*	*	*	*	*	*	*	1	1	1	0	1	SEL_ PWM CLK2	SEL_ PWM CLK1	SEL_ PWM CLK0

Figure 6. 89 CABC PWM Period control 1 Register (R6Bh)

SEL_PWMCLK[2:0]	CABC Mode
000	PWM_CLK / 1
001	PWM_CLK / 2
010	PWM_CLK / 4
011	PWM_CLK / 8
100	PWM_CLK / 16
101	PWM_CLK / 32
110	PWM_CLK / 64
111	PWM_CLK / 128

6.53 CABC PWM period control 2 Register (R6Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PWM_ Period7	PWM_ Period6	PWM_ Period5	PWM_ Period4	PWM_ Period3	PWM_ Period2	PWM_ Period1	PWM_ Period0
R	1	*	*	*	*	*	*	*	*	PWM_ Period7	PWM_ Period6	PWM_ Period5	PWM_ Period4	PWM_ Period3	PWM_ Period2	PWM_ Period1	PWM_ Period0

Figure 6. 90 CABC PWM Period control 2 Register (R6Ch)

Note: PWM_Period = (PWM_CLK) x (CLK Divier) x (PEM_Period + 1) x 255
Which, CLK Divier is mean SEL_PWMCLK[2:0] setting.

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6.54 CABC gain setting register (R6Fh ~ R77h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG06	BGG05	BGG04	BGG03	BGG02	BGG01	BGG00
R	1	*	*	*	*	*	*	*	*	0	BGG06	BGG05	BGG04	BGG03	BGG02	BGG01	BGG00

Figure 6. 91 CABC Gain setting Register (R6Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG16	BGG15	BGG14	BGG13	BGG12	BGG11	BGG10
R	1	*	*	*	*	*	*	*	*	0	BGG16	BGG15	BGG14	BGG13	BGG12	BGG11	BGG10

Figure 6. 92 CABC Gain setting Register (R70h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG26	BGG25	BGG24	BGG23	BGG22	BGG21	BGG20
R	1	*	*	*	*	*	*	*	*	0	BGG26	BGG25	BGG24	BGG23	BGG22	BGG21	BGG20

Figure 6. 93 CABC Gain setting Register (R71h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG36	BGG35	BGG34	BGG33	BGG32	BGG31	BGG30
R	1	*	*	*	*	*	*	*	*	0	BGG36	BGG35	BGG34	BGG33	BGG32	BGG31	BGG30

Figure 6. 94 CABC Gain setting Register (R72h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG46	BGG45	BGG44	BGG43	BGG42	BGG41	BGG40
R	1	*	*	*	*	*	*	*	*	0	BGG46	BGG45	BGG44	BGG43	BGG42	BGG41	BGG40

Figure 6. 95 CABC Gain setting Register (R73h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG56	BGG55	BGG54	BGG53	BGG52	BGG51	BGG50
R	1	*	*	*	*	*	*	*	*	0	BGG56	BGG55	BGG54	BGG53	BGG52	BGG51	BGG50

Figure 6. 96 CABC Gain setting Register (R74h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG66	BGG65	BGG64	BGG63	BGG62	BGG61	BGG60
R	1	*	*	*	*	*	*	*	*	0	BGG66	BGG65	BGG64	BGG63	BGG62	BGG61	BGG60

Figure 6. 97 CABC Gain setting Register (R75h)

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R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG76	BGG75	BGG74	BGG73	BGG72	BGG71	BGG70
R	1	*	*	*	*	*	*	*	*	0	BGG76	BGG75	BGG74	BGG73	BGG72	BGG71	BGG70

Figure 6. 98 CABC Gain setting Register (R76h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	BGG86	BGG85	BGG84	BGG83	BGG82	BGG81	BGG80
R	1	*	*	*	*	*	*	*	*	0	BGG86	BGG85	BGG84	BGG83	BGG82	BGG81	BGG80

Figure 6. 99 CABC Gain setting Register (R77h)

Note: Because CABC had differential Gain Curve under differential CABC mode. And then, the Gain Curve setting is from R6Fh to R77h.

Register	C[1:0]=01 (UI mode)	C[1:0]=10 (Still mode)	C[1:0]=11 (Moving mode)
R6Fh	24h	40h	40h
R70h	24h	3Ch	3Ch
R71h	24h	38h	38h
R72h	23h	34h	34h
R73h	23h	33h	33h
R74h	23h	32h	32h
R75h	22h	2Bh	2Dh
R76h	22h	24h	2Bh
R77h	22h	22h	28h

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7. Electrical Characteristic

7.1 Absolute maximum ratings

Item	Symbol	Unit	Spec.			Note
			Min.	Typ.	Max.	
Power Supply Voltage 1	VCC,IOVCC~VSSD	V	-0.3	-	+4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3	-	+4.6	Note(1),(2)
Power Supply Voltage 3	VLCD ~ VSSA	V	-0.3	-	+6.6	Note(3)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3	-	+4.6	Note(4)
Power Supply Voltage 5	VLCD ~ VCL	V	-0.3	-	+9	Note(5)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3	-	+18.5	Note(6)
Power Supply Voltage 7	VSSA ~ VGL	V	0	-	-16.5	Note(7)
Input Voltage	Vi	V	-0.3	-	VCC+0.3	-
Operating Temperature	Topr	℃	-40	-	+85	Note(8),(9)
Storage Temperature	Tstg	℃	-55	-	+110	Note(8),(9)

Note: (1) VCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure VLCD ≥ VSSA.
(5) To make sure VLCD ≥ VCL.
(6) To make sure VGH ≥ VSSA.
(7) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(8) For die and wafer products, specified up to +85℃.
(9) This temperature specifications apply to the TCP package.

7.2 ESD protection level

Mode	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	±2.0K	V
Machine Model	C = 200 pF, R = 0.0 Ω	±200	V

Table 7. 1 ESD Protection Level

7.3 Latch-up protection level

TBD

7.4 Light sensitivity

TBD

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7.5 Maximum series resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
P68, BS[2:0], IFSEL0, BURN, REGVDD,RES_SEL[1:0], BURN.	Input	100	Ω
NRD_E, NWR_RNW, DNC_SCL, NCS, SDI	Input	100	Ω
NRESET	Input	100	Ω
DB[17:0], DOTCLK, ENABLE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
VLCD	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Capacitor connection	30	Ω
VREG3	Capacitor connection	20	Ω
VCOMH, VCOML	Capacitor connection	20	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
VCOMR	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
VBGP, SDO, TE, NISD, PWM_OUT.	Output	100	Ω
DMY_IOVCC, DMY_GND, IOGNDDUM1-10	Output	10	Ω

Table 7. 2

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7.6 DC characteristics

(Vcc = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, T_A = -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Spec.			Note
				Min.	Typ.	Max.	
Input high voltage	V_{IH}	V	IOVcc= 1.65 ~ 3.3V	0.7xIOVcc	-	IOVcc	-
Input low voltage	V_{IL}	V	IOVcc= 1.65 ~ 3.3V	-0.3V	-	0.3xIOVcc	-
Output high voltage(1) (D0-17 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVcc	-	-	-
Output low voltage (D0-17 Pins)	V_{OL1}	V	IOVcc= 1.65 ~ 2.4V I_{OL} = 0.1mA	-	-	0.2xIOVcc	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ Vcc	-	1	-	-
Current consumption during normal operation (Vcc – VSSD)+ (IOVcc-VSSD)	$I_{OP(Vcc)}$	mA	Vci=IOVcc=Vcc=2.8V , Ta=25°C , GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=100, AP=100, FS0=00, FS1=11, BT=1000, VC1=111,VC2=100, VC3=000 VRH=0011, VCM=0100000,VDV=01110, VCOMG=1 With standard panel loading	-	1	-	-
Current consumption during normal operation (Vci – VSSD)	$I_{OP(Vci)}$	mA		-	11	-	-
Current consumption during standby mode (Vcc – VSSD) + (IOVcc-VSSD)	$I_{ST(VCC)}$	µA	Vcc=2.8V , Ta=25°C	-	6	20	-
Current consumption during standby mode (Vci – VSSD)	$I_{ST(VCi)}$	µA		-	1	1.5	-
Output voltage deviation	-	mV	0-Gray / 1-Gray 62-Gray / 63-Gray	-	40	-	-
	-	mV	2-Gray ~ 61-Gray	-	20	-	-

Table 7. 3 DC Characteristic

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7.7 AC characteristics

7.7.1 Parallel interface characteristics (8080-series MPU)

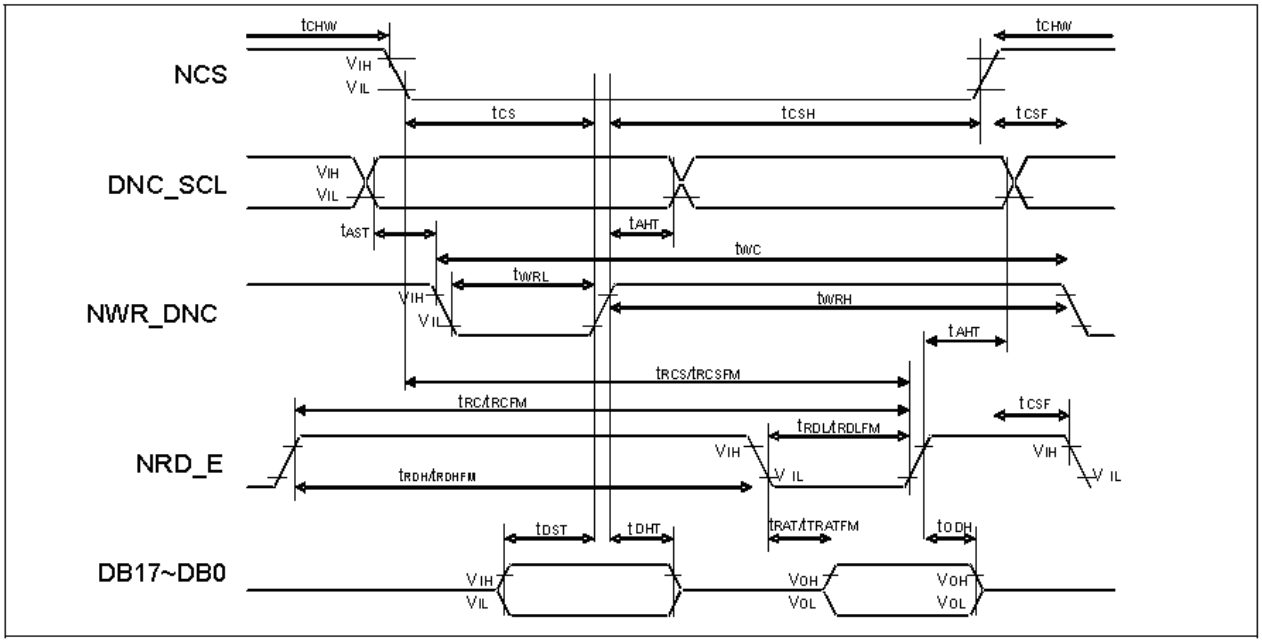

Figure 7. 1 Parallel Interface Characteristics (8080-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCC=2.3V TO 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70° C)

Signal	Symbol	Parameter	Spec. Min.	Spec. Max.	Spec. Unit	Description
DNC_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	-	ns	-
NCS	t_{CHW} t_{CS} t_{RCS} t_{RCSFM} t_{CSF} t_{CSH}	Chip select "H" pulse width Chip select setup time (Write) Chip select setup time (Read ID) Chip select setup time (Read FM) Chip select wait time (Write/Read) Chip select hold time	0 35 100 100 10 10	-	ns	-
NWR_RNW	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse "H" duration Control pulse "L" duration	100 20 20	-	ns	-
NRD_E (ID)	t_{RC} t_{RDH} t_{RDL}	Read cycle (ID) Control pulse "H" duration (ID) Control pulse "L" duration (ID)	150 40 50	-	ns	When read ID data
NRD_E (FM)	t_{RCFM} t_{RDHFM} t_{RDLFM}	Read cycle (FM) Control pulse "H" duration (FM) Control pulse "L" duration (FM)	250 50 150	-	ns	When read from frame memory
DB17~0	t_{DST} t_{DHT} t_{RAT} t_{RATFM} t_{ODH}	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	20 20 - - 20	- - 70 100 80	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) When normal operation, VDDD=1.65 ~ 2.0V, HX8352-A can meet above timing.

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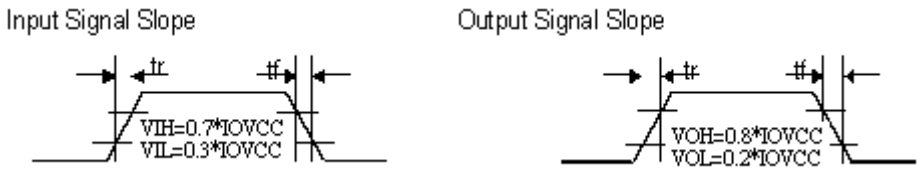

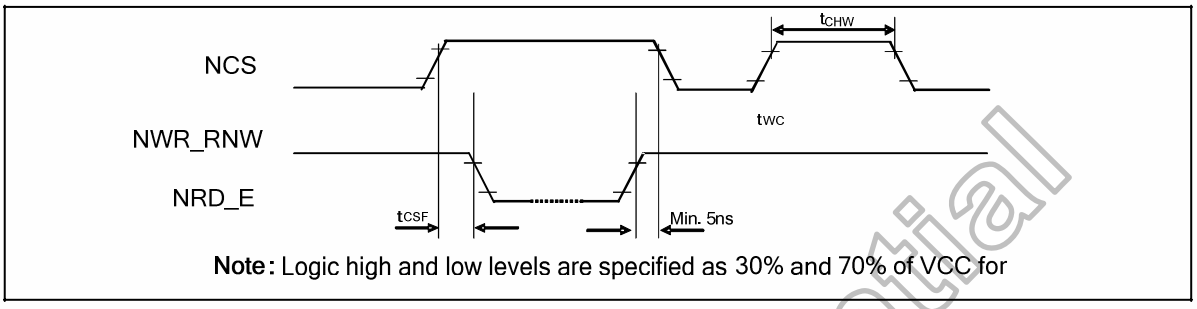

Figure 7. 2 Chip Select Timing

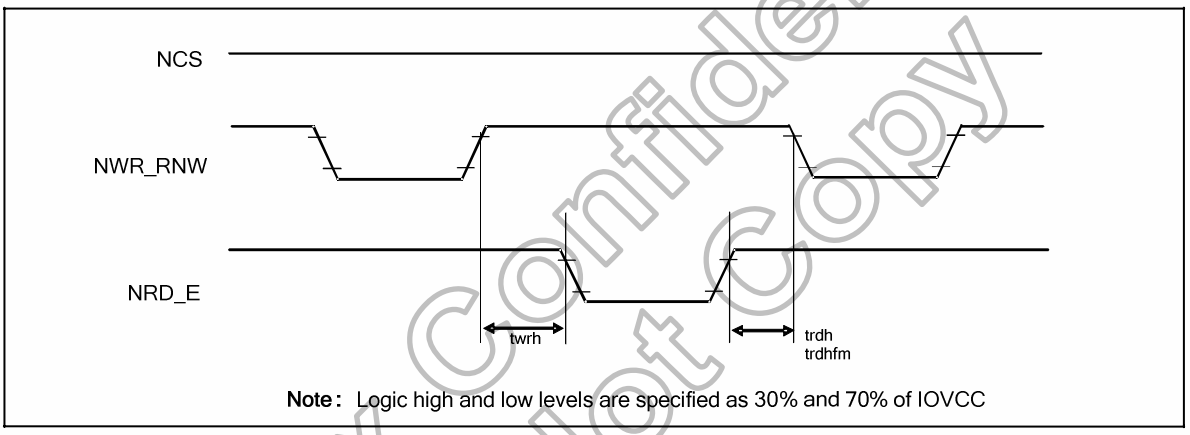

Figure 7. 3 Write to Read and Read to Write Timing

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7.7.2 Parallel interface characteristics (6800-series MPU)

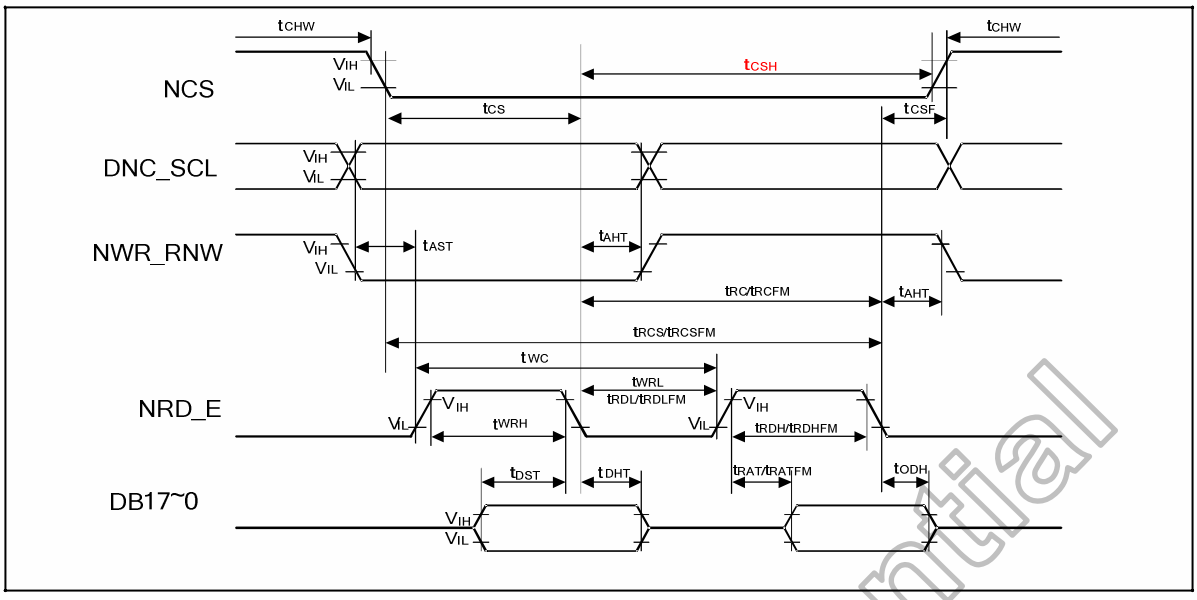


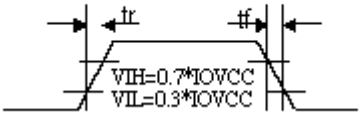
Figure 7. 4 Parallel Interface Characteristics (6800-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCC=2.3V TO 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70℃)

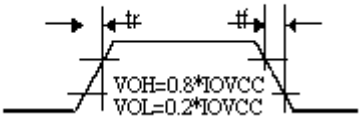
Signal	Symbol	Parameter	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Description
DNC_SCL	t_{AST}	Address setup time	10	-	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-	-		
NCS	t_{CHW}	Chip select "H" pulse width	0	-	-	ns	-
	t_{CS}	Chip select setup time (Write)	35	-	-		
	t_{RCS}	Chip select setup time (Read ID)	100	-	-		
	t_{RCSFM}	Chip select setup time (Read FM)	100	-	-		
	t_{CSF}	Chip select wait time(Write/Read)	10	-	-		
	t_{CSH}	Chip select hold time	10	-	-		
NWR_RNW	t_{WC}	Write cycle	100	-	-	ns	-
	t_{WRH}	Control pulse "H" duration	20	-	-		
	t_{WRL}	Control pulse "L" duration	20	-	-		
NRD_E (ID)	t_{RC}	Read cycle (ID)	150	-	-	ns	When read ID data
	t_{RDH}	Control pulse "H" duration (ID)	40	-	-		
	t_{RDL}	Control pulse "L" duration (ID)	50	-	-		
NRD_E (FM)	t_{RCFM}	Read cycle (FM)	250	-	-	ns	When read from frame memory
	t_{RDHFM}	Control pulse "H" duration (FM)	50	-	-		
	t_{RDLFM}	Control pulse "L" duration (FM)	150	-	-		
DB17~0	T_{dst}	Data setup time	20	-	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	20	-	-		
	t_{RAT}	Read access time (ID)	-	-	70		
	t_{RATFM}	Read access time (FM)	-	-	100		
	t_{ODH}	Output disable time	20	-	80		

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) When normal operation, VDDD=1.65 ~ 2.0V, HX8352-A can meet above timing.

Input Signal Slope



Output Signal Slope



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7.7.3 Serial interface characteristics

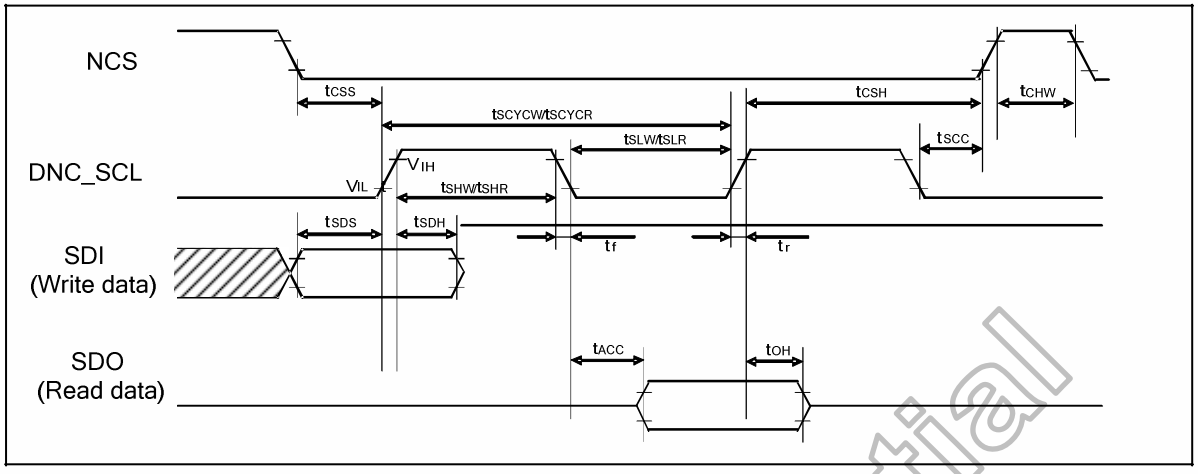
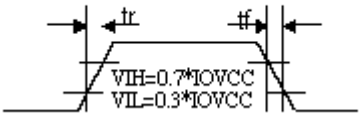


Figure 7. 5 Serial Interface Characteristics

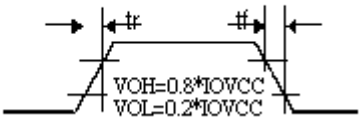
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Serial clock cycle (Write) DNC_SCL "H" pulse width (Write) DNC_SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	DNC_SCL	100 35 35	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDI	30 30	- -	- -	ns
Serial clock cycle (Read) DNC_SCL "H" pulse width (Read) DNC_SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	DNC_SCL	150 60 100	- - -	- - -	ns
Access Time	t_{ACC}	SDO for maximum C_L=30pF For minimum C_L=8pF	10	-	100	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For minimum C_L=8pF	15	-	100	ns
DNC_SCL to Chip select	t_{SCC}	DNC_SCL, NCS	50	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	45	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	NCS	60 60	- -	- -	ns

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) When normal operation, VDDD=1.65 ~ 2.0V, HX8352-A can meet above timing.

Input Signal Slope



Output Signal Slope



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7.7.4 RGB interface characteristics

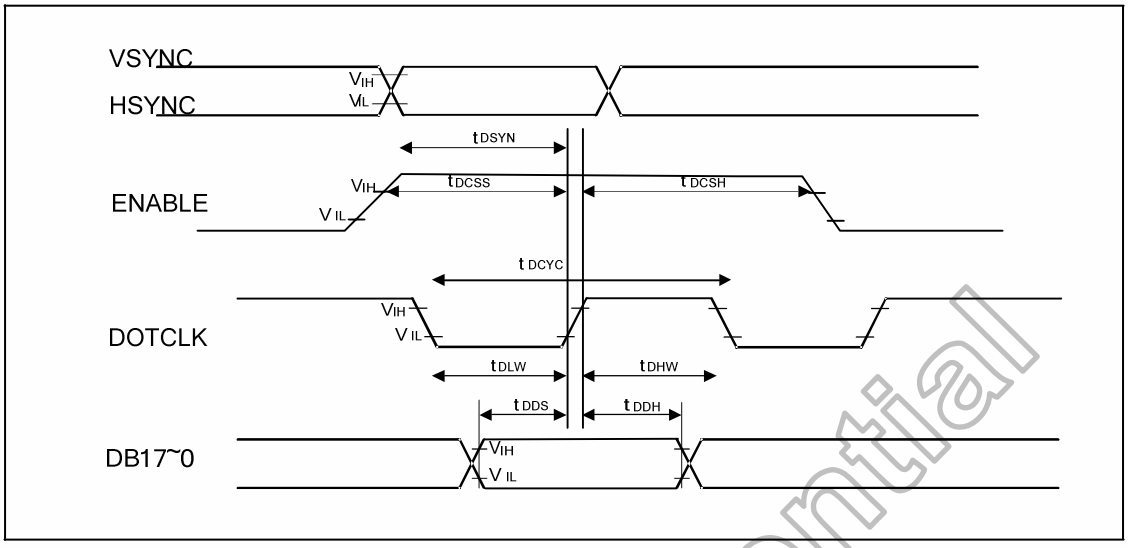


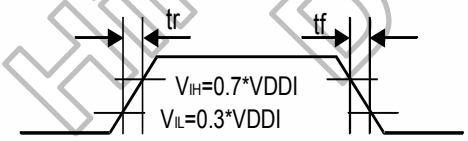
Figure 7. 6 RGB Interface Characteristics

Symbol	Parameter	Conditions	Related Pins	Spec.			Unit
				Min.	Typ.	Max.	
t_{DCYC}	DOTCLK cycle time	-	DOTCLK	100	-	-	ns
t_{DLW} t_{CHW}	DOTCLK Low time DOTCLK High time	-		20 20	- -	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	DOTCLK, DB17~0	15 15	- -	- -	ns
t_{DCSS} t_{DCSH}	ENABLE setup time ENABLE hold Time	-	ENABLE	15 15	- -	- -	ns
t_{DSYN}	SYNC setup time	-	DOTCLK, HSYNC, VSYNC	15	-	-	ns

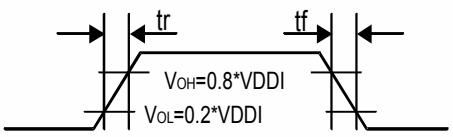
Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) The frequence of DOTCLK does not limited by frame rate.

Table 7. 4 RGB Interface Characteristics

Input Signal Slope



Output Signal Slope



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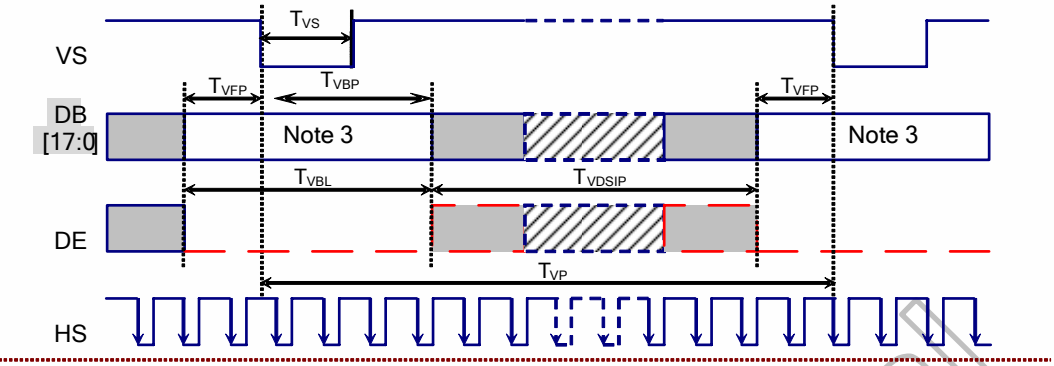
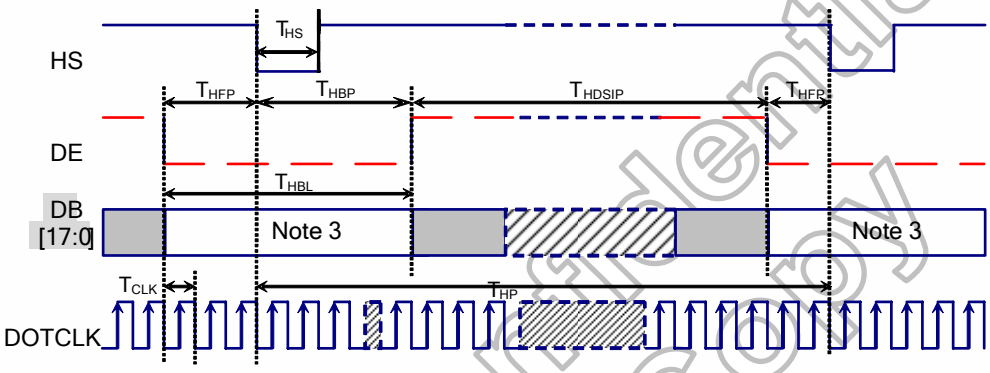
Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F



Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}		484	488	496	HS
Vertical low pulse width	T_{VS}		2	2		HS
Vertical front porch	T_{VFP}		2	4		HS
Vertical back porch	T_{VBP}		2	4		HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	4	8	16	HS
Vertical active area	T_{VDISP}			480		HS
						HS
						HS
Horizontal Timing						
Horizontal cycle period	T_{HP}		250	256	290	DOTCLK
Horizontal low pulse width	T_{HS}		2	4		DOTCLK
Horizontal front porch	T_{HFP}		5	8		DOTCLK
Horizontal back porch	T_{HBP}		5	8		DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{HFP}$	10	16	50	DOTCLK
Horizontal active area	T_{HDISP}			240		DOTCLK
Pixel clock cycle	f_{CLKCYC}			7.5	10.0	MHz

Note 1. IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
Note 2. HP is multiples of DOTCLK.

Table 7. 5 Vertical and Horizontal Timing for RGB I/F

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7.7.5 Reset input timing

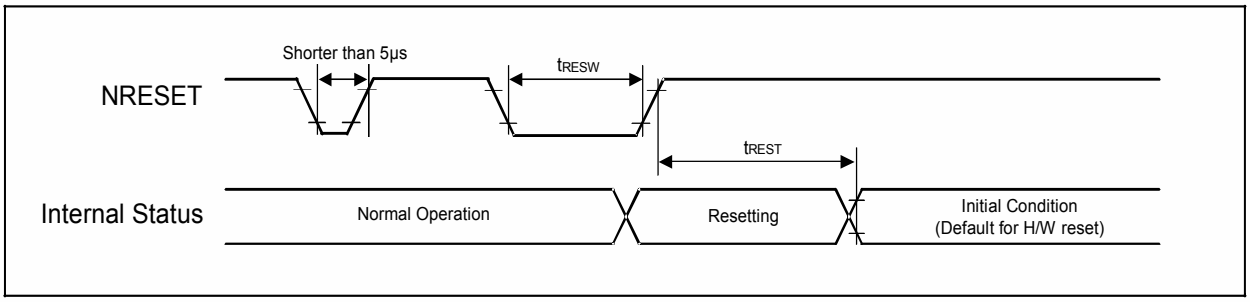


Figure 7. 7 Reset Input Timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during "Sleep In mode"	ms
		-		-	120	When reset applied during "Sleep Out mode"	ms

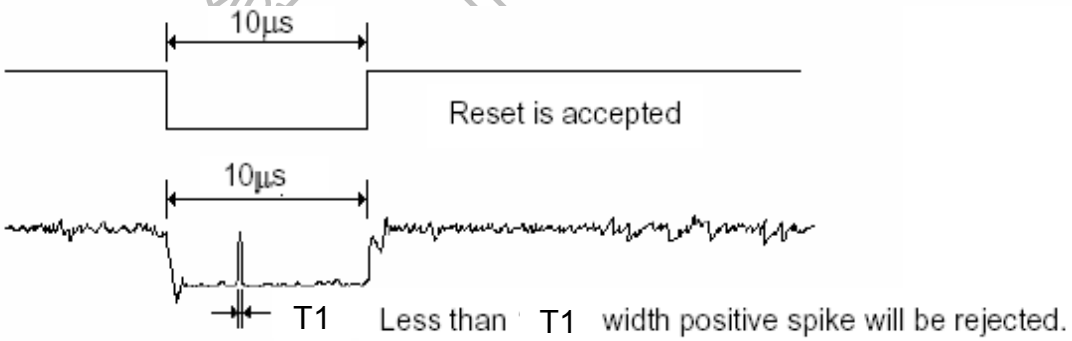
Note: (1)Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5µ	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

(2)During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Standby out –mode. The display remains the blank state in Standby In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of !RES.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
T1	Noise of spike	NRESET	200(1)	-	100(2)	-	ns

Note: (1) Min is mean IOVCC as 1.65V.
(2) Max is mean IOVCC=3.3V.
(3) It is necessary to wait 5msec after releasing !RES before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 7. 6 Reset Input Timing

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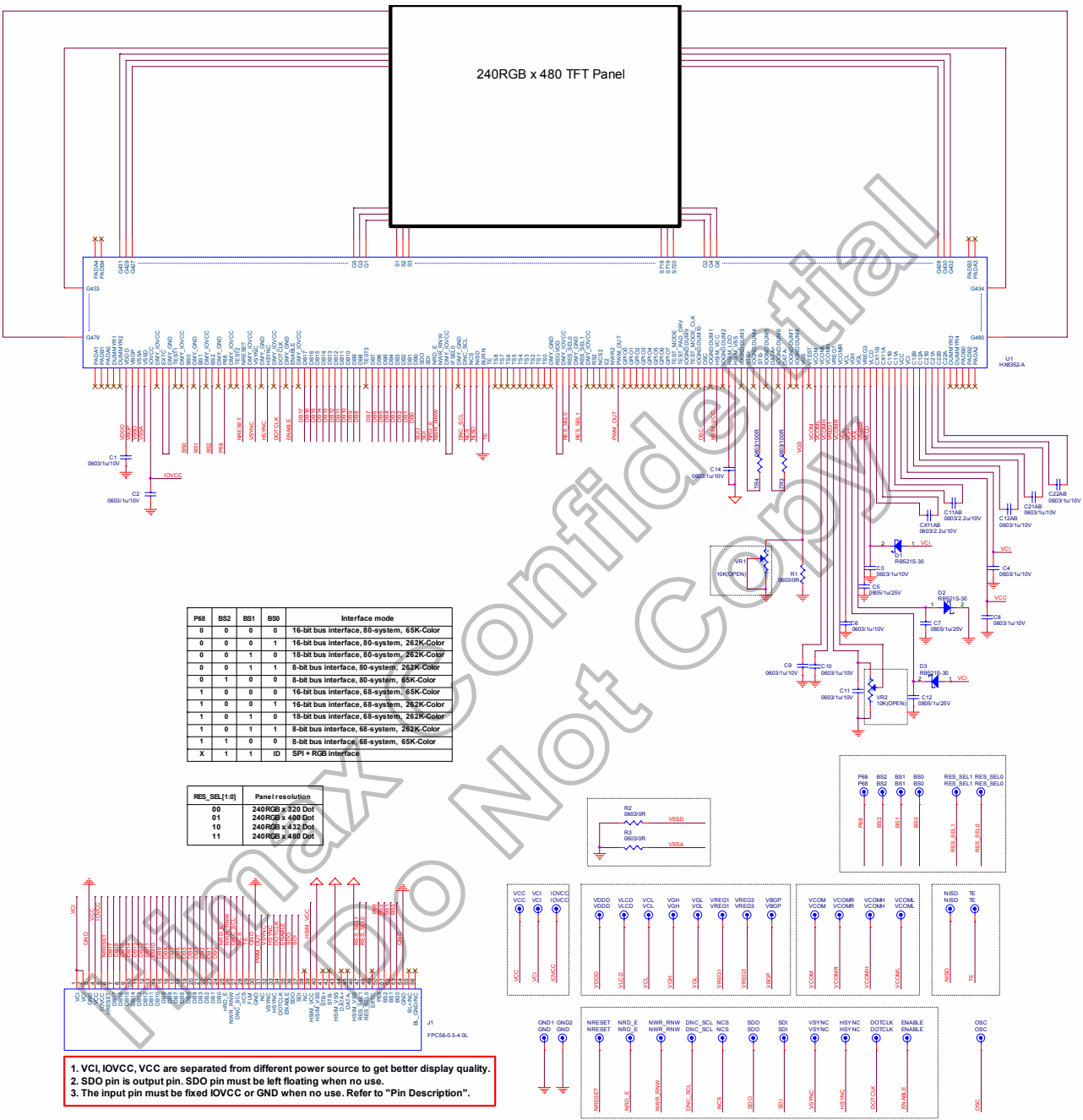
8. Reference Applications

8.1 Register- content interface mode



P68	BS2	BS1	BS0	Interface mode
0	0	0	0	16-bit bus interface, 80-system, 65K-Color
0	0	0	1	16-bit bus interface, 80-system, 262K-Color
0	0	1	0	18-bit bus interface, 80-system, 262K-Color
0	0	1	1	8-bit bus interface, 80-system, 262K-Color
0	1	0	0	8-bit bus interface, 80-system, 65K-Color
1	0	0	0	16-bit bus interface, 68-system, 65K-Color
1	0	0	1	16-bit bus interface, 68-system, 262K-Color
1	0	1	0	18-bit bus interface, 68-system, 262K-Color
1	0	1	1	8-bit bus interface, 68-system, 262K-Color
1	1	0	0	8-bit bus interface, 68-system, 65K-Color
X	1	1	ID	SPI + RGB interface

RES_SEL[1:0]	Panel resolution
00	240RGB x 320 Dot
01	240RGB x 400 Dot
10	240RGB x 432 Dot
11	240RGB x 480 Dot

1. VCI, IOVCC, VCC are separated from different power source to get better display quality.
2. SDO pin is output pin. SDO pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

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8.2 External components connection

Pad Name	Connection	Typical Capacitance Value
VCOMH	Connect to Capacitor (Max 6V): VCOMH---(+)----| |--- (-)------ VSSA	1.0µF
VCOML	Connect to Capacitor (Max 3V): VCOML ---(-)----| |--- (+)----- VSSA	1.0µF
VGL	Connect to Capacitor (Max 16V): VGL ---(-)----| |--- (+)----- VSSA	1.0µF
VGH	Connect to Capacitor (Max 21V): VGH ---(+)----| |--- (-)----- VSSA	1.0µF
VCL	Connect to Capacitor (Max 5V): VCL ---(-)----| |--- (+)----- VSSA	1.0µF
C22A,C22B	Connect to Capacitor (Max 7V): C22A ---(+)----| |--- (-)-----C22B	1.0µF
C21A,C21B	Connect to Capacitor (Max 7V): C21A ---(+)----| |--- (-)-----C21B	1.0µF
CX11A,CX11B	Connect to Capacitor (Max 7V): CX11A ---(+)----| |--- (-)-----CX11B	2.2µF
C11A,C11B	Connect to Capacitor (Max 5V): C11A ---(+)----| |--- (-)-----C11B	2.2µF
C12A,C12B	Connect to Capacitor (Max 6V): C12A ---(+)----| |--- (-)-----C12B	1.0µF
VREG1	Connect to Capacitor (Max 6V): VREG1 ---(+)----| |--- (-)-----VSSA	1.0µF
VREG3	Connect to Capacitor (Max 7V): VREG3 ---(+)----| |--- (-)-----VSSA	1.0µF
VDDD	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0µF
VLCD	Connect to Capacitor (Max 6V): VLCD ---(+)----| |--- (-)-----VSSA	1.0µF
VCI	Connect to Capacitor (Max 6V): VCI ---(+)----| |--- (-)-----VSSA	2.2µF
VCC	Connect to Capacitor (Max 6V): VCC ---(+)----| |--- (-)-----VSSA	2.2µF
IOVCC	Connect to Capacitor (Max 6V): IOVCC ---(+)----| |--- (-)-----VSSA	1.0µF

Note: The above mentioned capacitors must be connected; otherwise it will cause poor display quality.

Table 8. 1 Connect Capacitors

Component	Specification	Remarks
Diode	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: HSC226)	Connect to Schottky Diode
Variable Resistor (VCOMR)	> 200KΩ	Connect to variable resistor while the VcomH1 is adjusted by external voltage input.

Note: The above mentioned components must be connected; otherwise it will cause poor display quality.

Table 8. 2 Connected Schottky Diode and Resistor

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9. Ordering Information

Part No.	Package
HX8352-A000 PDxxx	PD : mean COG xxx : mean chip thickness (μm), (default: 300 μm)

10. Revision History

Version	Date	Description of Changes
01	2007/04/30	New setup
	2007/05/08	Update PAD coordinates.
	2007/05/10	1. Update 3. Block Diagram. 2. Update DB17~DB0 pin describe in 4.1 Pin Description 3. Modify Figure 6.93 ABC DUTY Control Register. 4. Update Table 7.2.
	2007/05/16	1. Change Figure 5.39 Index data from 00202h to 00804h. 2. Change Figure 5.40 Index data from 00202h to 00804h.
	2007/05/21	Update OTP Memory table.
	2007/05/30	1. Modify Pin number from 435 to 447 in 4.2 Pin Assignment 2. Modify Pin name in Figure 5.1 ~ 5.6.
	2007/06/01	Modify 4.1-Au Bump Size.
	2007/07/20	1. Update Gamma formula 2. Modify Figure 5.78 Gamma Resister Stream and Gamma Reference Voltage. 3. Update Table 5.18 Output Voltage of 8 to 1 Selector. 4. Update Command set
	2007/08/16	1. Add terminal resistance of 8.2 High speed Interface mode reference applications.
	2007/09/06	1. Modify Table 5. 32 EPL Bit Setting and Valid Enable Signal. 2. Modify description of EPL polarity in P150. 3. Modify description of R08h~R09h in P124. 4. Modify description of R22h (Write Data register) in P139. 5. Updated Figure 5. 89 Display On/Off Set Sequence. 6. Modify description of R53h in P67. 7. Modify description of R4F in P62. 8. Updated Reference Application circuits in P172~P173. 9. Modify description of Table 5.29 OTP Memory table. 10. Updated Figure 5.86 OTP Progrmming Flow. 11. Updated OTP Programming Sequence in P116. 12. Modify description of R25h ~ R2Ah in P143.
	2007/09/19	1. Modify description of Register Access Packet in P53.
	2007/10/29	1. Modify Pin Description of High speed part in P14~P15.
	2007/11/01	1. Modify OTP table in P114. 2. Modify register table in P120. 3. Add new register (R00h) in P122. 4. Modify RTN table in P146. 5. Add Value of AC Characteristics in P166 ~ P170.
	2007/11/21	1. Modify R56h ~ R59h index value in P158~P159. 2. Modify step 14 of PROGRAM SEQUENCE in P116. 3. Modify description of IDMON in P122.

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	200712/24	1. Modify pin description in P15. 2. Add new register R95h, R96h andR97h in Register table in p121. 3. Modify N_SAP table in P151. 4. Modify description of R5Ch in P160. 5. Add new register R95h, R96h andR97h in P161-P162. 6. Modify Splike rejection of Reset input timing in P173.
02	2008/01/09	1. Remove SPI Write GRMA timing In P44. 2. Modify OTP table in P112. 3. Modify AC Characteristics in P164 ~ P168.
	2008/03/11	1. Add new register R83h in P159. 2. Add new register R85h in P159. 3. Add new register R8Bh and R8Ch in P160. 4. Modify description of R95h in P161. 5. Modify description of R97h in P162.
03	2008/03/21	1. Modify OTP table in P112.
	2008/05/09	1. Remove High speed Interface. 2. Add new register (R6Fh ~ R77h).
04	2008/08/12	1. Remove preliminary in the datasheet.
05	2008/12/24	1. Modify description of RES(1-0) setting in P12. 2. Modify R1Bh (AP table) in P98. 3. Add new register R8Ah in P123. 4. Add R6Bh and R6Ch (PWM period control setting register) in P125. 5. Add table 7.5 porch setting of RGB IF in P136.

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